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Advanced Control of Single-Phase Inverters for Microgrid Integration.

SUMMARY

Scientific supervisor

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Having reached the end of this PhD journey, I would like to express my sincere gratitude to those who supported me along the way

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Table of Contents

1. INTRODUCTION

1.1 BACKGROUND AND MOTIVATION

A significant proportion of residential-scale renewable energy installations such as photovoltaic (PV) systems rely on single-phase inverters. Effective control of these inverters is therefore crucial, for example, in managing the second order oscillations, inherent in the DC-link of single-phase inverters. If these oscillations are not decoupled from the DC side, they could have adverse effects on the performance of the primary source. The effects include, overheating of batteries in battery energy storage systems, increase of thermal stress on the DC-link capacitors and reduction in conversion efficiency in PV systems [1], [2]. To solve this challenge, active power decoupling (APD) methods have been proposed as a viable solution [3], [4], [5]. APD methods rely on redirecting these oscillations from the DC side to other processing elements. Through APD methods the capacitance requirements of the DC-link can also be significantly reduced, allowing for the replacement of bulky electrolytic capacitors with thin-film capacitors that offer higher lifetime. Various topologies have been proposed in literature to achieve APD. The majority of these topologies involve implementing an additional circuit to the main inverter circuit to process the low-frequency oscillations [6], [7]. These topologies, however, result in additional costs associated with the additional semiconductor components and gate driver circuits. To avoid this drawback, differential single-phase inverters have been proposed [8], [9]. The benefits of achieving APD while keeping the number of additional components minimal motivated this thesis to undertake a comprehensive study on this class of inverters.

Microgrids (MGs) provides an ideal framework for integrating various inverter based distributed energy resources (DERs) such as PV systems and battery energy storage units. These MGs can operate either in islanded or grid connected mode [10], [11]. Within MGs, inverters act as the primary interface for DERs, allowing them to deliver active and reactive power while maintaining voltage and frequency stability. Currently, most of the grid connected inverters operate as grid-following (GFL), relying on an external voltage source such as the grid to synchronize on [12] . While GFL control is effective for strong grids, it suffers from stability issues in weak grids [13]. This challenge becomes critical under high renewable penetration, due to reduced system inertia and increased effective network impedance which makes the grid weak [14]. In such scenarios, inverters must be able to operate autonomously while maintaining stability. To address this challenge most research now focuses on grid-forming (GFM) control [15]. Unlike GFL, GFM inverter is able to establish its own terminal voltage and frequency, enabling MGs to maintain stable operation even in low-inertia environments, while disconnected from the local grid. Several GFM strategies have been developed, that includes droop control, virtual synchronous machine (VSM), and more recent methods based on virtual oscillator control (VOC) [16], [17]. The advantages provided by VOC, such as faster synchronization and faster transient response, gave motivation to study VOC based primary control with a focus on single-phase systems.

While primary control ensures voltage and frequency regulation for each inverter, steady-state deviations will still exist after a disturbance [18]. This higher-level task of restoring voltage and frequency to nominal is assigned to secondary control. In general, the secondary control methods can be categorized into centralized, distributed and decentralized [19] . Centralized method suffers from a single point of failure as well as scalability challenges while decentralized control methods that

operates only based on local measurements may have suboptimal performance due to lack of proper coordination [20]. Due to the distributed structure of MG which typically consists of independent and spatially dispersed units, distributed secondary control provides an effective way to regulate voltage and frequency while improving on scalability and resilience [21]. This has provided motivation for this thesis to develop and implement distributed secondary control methods which are compatible with VOC. The focus was on distributed secondary control based on distributed averaging and consensus methods.

1.2 NECESSITY AND JUSTIFICATION OF THE THESIS

The urgency to address climatic change while meeting the global energy demand has led to an increasing shift from fossil fuels to renewable energy sources (RES) [22], [23]. MGs are a key enabler of this transition, being able to aggregate various DERs and loads into a controllable unit [24]. The ability of GFM inverters to operate autonomously, establishing and maintaining voltage and frequency without relying on an external grid makes them ideal for islanded MG. VOC is one of the GFM control strategies that has recently gained attention due to its self-synchronization and advanced control capabilities [25]. Two nonlinear VOC models, the Van-der-Pol and Andronov-Hopf Oscillator (AHO) are presented in this thesis. Despite its advantages, existing VOC control methods lack mechanisms for power limitations and robust secondary control methods. This thesis addresses this gap, by developing a control structure that integrates power limitation and distributed secondary control layers into a VOC-based framework. Power limitation controller dispatches power according to the operating conditions and the primary source availability. Therefore, this mechanism allows the inverter to adapt to the intermittent nature of RES and the operational constraints of batteries. The controller can limit both active and reactive power to specified setpoints and when the inverter reaches its power limit, the others that are not restricted by the power limitation take on the extra load. In addition, the secondary control was formulated using distributed control strategies i.e. averaging and consensus-based approaches. The developed secondary control methods can regulate both voltage and frequency as well as maintaining power sharing according to the available power in the primary source. In addition, robustness against the effects of clock drifts, inherent in digital controllers, was also considered when designing the secondary control strategy.

Over the last decade, research in the field of single-phase inverters has gained significant attention, mainly driven by the need to develop more efficient, reliable, and cost-effective RES applications. However, despite recent advancements in both control and hardware solutions, the adoption of high-speed switches (i.e., silicon carbide (SiC)/gallium nitride (GaN) semiconductors) and the necessity to implement advanced control techniques have introduced new technical challenges. One significant issue related to migration to new technologies is system lifespan extension. Specifically, in PV applications, improving the reliability of inverters is crucial for reducing the current disparity between their lifespan (typically 10–15 years) and that of PV panels (20-25 years) [26] , [27]. One objective is to extend the inverter lifespan to match that of the PV panels. Consequently, this thesis focuses on the latest single-phase inverter topologies that prioritize a minimalist hardware design for APD purposes, with the use of highly reliable components, particularly film capacitors.

This research aligns with the United Nations Sustainable Development Goal (SDG) 7, aimed at ensuring access to affordable, reliable, sustainable and modern energy for all [28]. Similarly, the European Green

deal has set an ambitious target to become climate neutral by 2050 [29], both highlighting the importance of renewable energy and resilient power system.

1.3 AIM AND OBJECTIVES

This research aims to develop, analyze, and validate advanced control strategies for single-phase inverters to improve their reliability and performance for integrating into an MG.

The objectives of this thesis are outlined as follows:

- Analyzing various differential single-phase inverters proposed in the literature (divided into three main classes: buck, boost, and buck-boost) and derive the optimal topology based on the parameters and indices such as switch voltage and current stresses, switch utilization, and losses.
- Developing a unified mathematical description of each topology to allow an easier evaluation of the inverters' operational limits under different parameters.
- To identify and discuss the main APD control strategies and their implementation. The main emphasis being on autonomous control algorithms that minimize dependency on system parameters.
- To develop advanced control methods for single-phase inverters based on VOC, enabling fast synchronization, improved transient response, stable voltage and frequency regulation under MG conditions.
- To integrate APD control with advanced control based on VOC for improved performance of single-phase inverters within an MG.
- To design and develop distributed secondary control methods for voltage and frequency restoration and power sharing. The methods are designed to ensure that they are resilient to clock drifts which are inherent in digital controllers.
- To develop and validate power limitation strategy for VOC-based inverters, enhancing their operation withing an MG environment. A power limitation controller that dispatches power according to the operating conditions and the primary source availability, allowing the inverter to adapt to the intermittent nature of RES and the operational constraints of batteries.
- To verify the effectiveness of the developed control approaches through simulations and extensive experiments performed using laboratory-scale MG setups.

1.4 STRUCTURE OF THE THESIS

The thesis is organized into seven chapters:

Chapter 1: Introduction — introduces the background and motivation of research. Firstly, challenges of second order oscillations in the DC-link of single-phase inverter systems are highlighted and the need for effective control solutions to manage these oscillations. APD control methods have been proposed as a viable option, given their advantages of minimizing the DC-link capacitance requirements. More emphasis was given to those topologies that use the minimum number of components to achieve APD. After that, the chapter then discusses the broader context of integrating single-phase inverters into MGs environments and the weak and low-inertia nature of MGs, which

necessitates reliable GFM control to maintain stable voltage and frequency. The chapter also provides justification for the research and concludes by presenting the overall aim and objectives of the thesis.

Chapter 2: Differential single-phase inverter topologies with APD and optimal topology derivation — provides state-of-the-art analysis, including the main topologies that are used to achieve APD with the minimum number of components as well as the control methods. In addition to the state of the art, the chapter incorporates unified mathematical descriptions and analytical results developed as part of this research for each examined topology, allowing an easier evaluation of the inverters operational limits under different parameters.

Chapter 3: Control of a single-phase differential inverter and its integration with advanced control based on Van der Pol VOC for MG integration — presents the development of advanced control framework for single-phase inverters based on Van der Pol oscillator primary control. The chapter focuses on the standalone operation of a single inverter to establish VOC core control principles before its integration into an MG in subsequent chapters. Both conventional and inverse VOC control schemes are presented, and the steady-state and dynamic performances are conducted under linear and nonlinear loading conditions.

Chapter 4: Control of single-phase islanded MG based on Van der Pol VOC enhanced with power limitation and robust distributed secondary control — Building on the primary control principles of the Van der Pol VOC established in Chapter 3, this chapter focuses on the integration of multiple inverters in an MG. It then presents a power limitation strategy that can limit both active and reactive power to specified setpoints, enhancing the operation of VOC based inverters. Finally, a distributed secondary control scheme based on averaging is presented to restore voltage and frequency to nominal, as well as ensuring power sharing among inverters.

Chapter 5: Andronov-Hopf-oscillator based control of an islanded MG with distributed consensus secondary control — This chapter extends the study of VOC by presenting an MG with a control framework derived from the Andronov-Hopf oscillator. This was motivated by the advantages provided by this oscillator of generating signals with less harmonic components compared to the Van der Pol oscillator. After that, a consensus-based distributed secondary control framework designed to be compatible with AHO-based GFM inverters is presented for restoring voltage and frequency as well as maintaining power sharing.

Chapter 6: Development of experimental platforms for MG applications — this chapter presents the experimental platforms, both HIL setup and setup with physical inverters used to validate the MG control strategies developed throughout the thesis. The experiments were carried out at the R&D Institute of Transilvania University of Brasov and at Aalborg University.

Chapter 7: Conclusion — provides the conclusions of the thesis by summarizing the key findings, contributions, future research directions and dissemination of research results.

2. DIFFERENTIAL SINGLE-PHASE INVERTER TOPOLOGIES WITH ACTIVE POWER DECOUPLING AND OPTIMAL TOPOLOGY DERIVATION

The content of this chapter has been published by the author in IEEE Access , vol. 11, 2023 [30] and in the proceedings of the 2023 International Aegean Conference on Electrical Machines and Power Electronics (ACEMP) & 2023 International Conference on Optimization of Electrical and Electronic Equipment (OPTIM) [31].

As an important segment of power electronics, single-phase inverters are widely used today in a variety of small-scale applications (i.e. kW range), such as RES, on-board chargers of electric vehicles, home appliances, or uninterruptible power supplies [32], [33], [34]. Consequently, there has been increased research interest in both hardware topologies and control solutions for single-phase inverters, with a focus on improving reliability, reducing costs, increasing efficiency, and enhancing power density [35], [36], [37]. The adoption of wide-bandgap semiconductors, such as SiC and GaN, which have been proven to outperform traditional silicon-based transistors (at least in small-scale applications) by higher voltage and temperature ratings, faster switching speeds, and lower losses [38], [39], [40], [41], represents an important path towards achieving the aforementioned goals.

Another major challenge in single-phase inverters is the processing of the inherent second-order power oscillation component, which needs to be prevented from being transferred to the DC source [8], [42], [43]. The processing of these low-frequency oscillations requires high energy storage. Conventionally, passive decoupling techniques that utilize large DC-link electrolytic capacitors have been used. However, because of the relatively short lifetime of electrolytic capacitors, also highly dependent on temperature [44], [45], [46] other solutions have been investigated in literature which are commonly referred to as APD techniques [7], [3], [47], [48], [49]. The main idea behind APD solutions is to direct the power oscillations to a more reliable short-term energy storage element, such as thin film capacitors, which is referred to as the decoupling capacitors.

Two different techniques are commonly used in APD methods to transfer pulsating power to a buffering component. The first involves adding active switches to the converter circuit, such as a third leg [50], [51], [52] and the second does not add any additional active elements. The use of extra semiconductor devices to achieve power decoupling affects the power density, cost, and efficiency of the converter [53], [54]. Therefore, differential inverters are a suitable option for achieving APD without the need for additional semiconductor components. Because of their small component count, they offer a cost-effective solution for handling the second-order ripple component in single-phase inverters.

The general structure of a voltage source differential single-phase inverter is illustrated in Fig 1 [30]. It consists of two half-bridge (HB) converters (A and B) that operate in either differential mode (DM) or common mode (CM). The DM transfers power from the input port (DC) to the output port (AC), and the CM can be used to achieve APD. Each HB is a DC-DC converter that can be configured as a buck, boost, or buck-boost topology. Starting from these basic topologies, different inverter topologies can be identified, namely differential buck (DBU), differential boost (DBO), differential buck-boost (DBB), and differential buck inverters with split capacitors on the AC side (DBU-SC). In addition, other topologies

to achieve APD, such as an H-bridge with a DC split capacitor (DSCHB) and its reduced switch inverter (RS-DSCHB), are also considered.

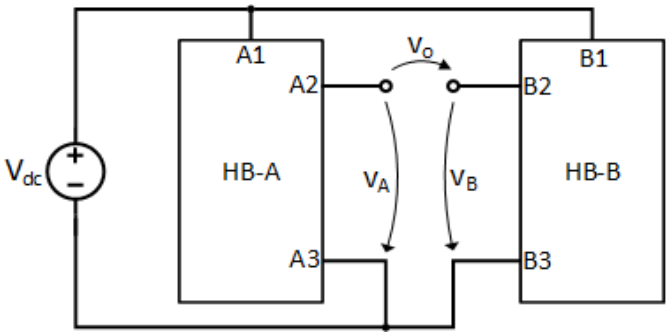


Fig 1. Generic structure of single-phase differential inverters.

2.1 DIFFERENTIAL SINGLE-PHASE INVERTER TOPOLOGIES

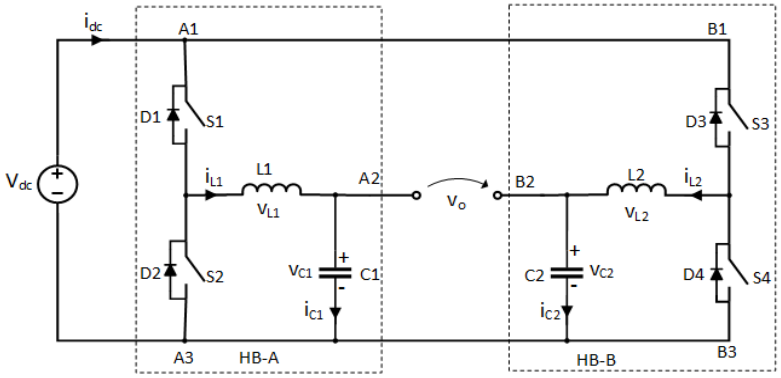
As illustrated in Fig 1, the general structure of a voltage source differential single-phase inverter consists of two synchronous HB (HB-A and HB-B) supplied by a common DC source [30]. The inverter supports two modes of operation; DM and the CM. DM is the primary mode for delivering power from the input port (DC) to the output port (AC). The CM operation can be used for other purposes such as APD control. A synchronous HB inverter has two switches that operate in a complementary manner and a filter inductor connected to the midpoint. A filter capacitor is also added to the output to provide low pass filtering together with the inductor. HB-A and HB-B are connected in parallel to the same DC input source, and each HB is modulated such that the differential output voltage across the two HB is sinusoidal. This generic topology is configurable, and depending on the component arrangement, it can be configured to implement one of three fundamental topologies: buck, boost, or buck-boost.

A timeline of the analyzed differential inverter topologies with APD, with the main references that provided a new approach that led to the development of the considered topology, is shown in Table 1. The vertical axis represents the topology as defined in this study, whereas the horizontal axis represents the year in which the reference was published, as well as the types of decoupling controllers and loads (linear/nonlinear, autonomous operation, or grid-connected). As shown in Table 1, most of the contributions were made to the DBU inverter, which was found to be the most practical, as also revealed in this chapter.

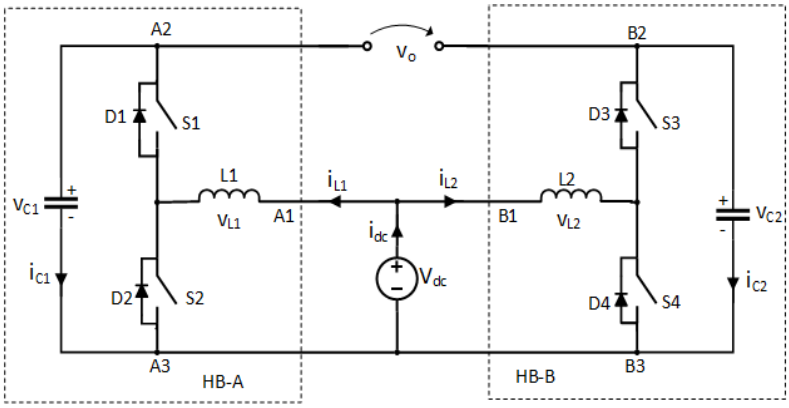
Fig 2(a) to Fig 2(c) show the schematics of the DBU inverter, DBO, and DBB, respectively. The midpoint between the two decoupling capacitors, C_1 and C_2 is connected to the negative terminal of the DC source. A similar operation is obtained if the common point of the decoupling capacitors is connected to the positive rail. The two terminals, $A_2$and B_2, on the AC side are then connected differentially across the load or grid.

Table 1: A timeline of the active power decoupling topologies for differential inverters.

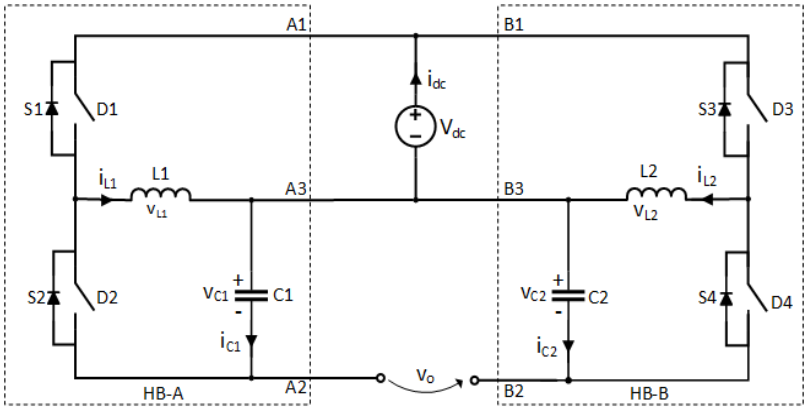
Topology	Publication year												Decoupling controller	Load type
	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	
DBU	[55]												Analytical reference generation	Linear
			[8]										Multi resonant	Linear
			[56]										Multi resonant	Grid
			[57]										HPF + PR	Linear
			[53]										HPF + PR	Grid
			[58]										Multi resonant	Grid/ Linear
			[59]										HPF + PR	Linear
				[60]									Multi resonant	Grid
						[9]							Multi resonant	Linear / nonlinear
								[61]					Multi resonant	Linear
									[62]				Analytical reference generation	Grid
									[63]				Multi resonant	Linear / nonlinear
										[43]			Multi resonant	Linear
										[64]			Multi resonant	Linear
										[65]			Multi resonant	Linear
										[66]			Multi resonant	Linear
											[31]		Multi resonant	Linear
											[67]		SOGI + Resonant	Grid
												[68]	SOGI + Multi resonant	Grid
													[69] Multi resonant	Grid
DBO			[59]										HPF + PR	Linear
			[70]										Bandpass filters	Grid
			[71]										Rule based controller	Grid
				[72]									Analytical reference generation	Linear
						[9]							Multi resonant	Linear / nonlinear
										[73]			Multi resonant	Linear / nonlinear
											[1]		Fractional order notch filter	Linear / nonlinear
DBB			[59]										HPF + PR	Linear
					[74]								Analytical reference generation	Linear
						[9]							Multi resonant	Linear /nonlinear
						[75]							Analytical reference generation	Linear
						[76]							HPF + Even frequency repetitive controller	Nonlinear
DBU-SC										[77]			Analytical reference generation	Linear
DSCHB	[78]												PR	Grid
				[42]									Multi resonant	Grid
							[79]						Total sliding mode controller	Grid
									[80]				Analytical reference generation	Linear
RS-DSCHB	[81]												PR	Grid
			[82]										Multi resonant	Grid / Linear



(a)



(b)



(c)

Fig 2. Differential single-phase inverters: (a) buck; (b) boost; (c) buck-boost.

Other topologies can be generated from these fundamental topologies, as in [77], in which the initial decoupling capacitors on the AC side of the DBU inverter are divided into two symmetrical forms. Fig 3 shows DBU-SC. In [83] , the midpoint of the two decoupling capacitors was connected to the midpoint of the split DC-link capacitor. Thus, the utilization of decoupling capacitors is improved. The output voltage of the differential single-phase inverter, as shown in Fig 1, is generated as a differential component between the two output ports of the two HB (A_2, B_2).

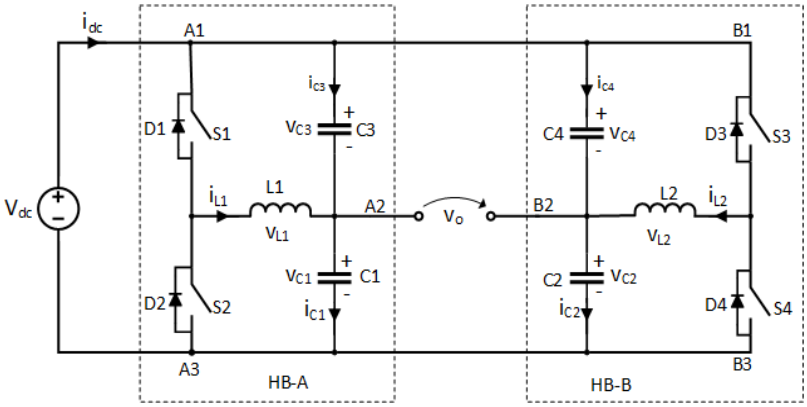


Fig 3. Differential buck with split capacitor on the AC side.

Without power decoupling, the two HB output voltages are controlled to follow the references shown in (1) with the same magnitude and frequency but 180° out of phase.

$$\begin{cases} v_A = V_d + 0.5V_m sin\,(\omega t) \\ v_B = V_d - 0.5V_m sin\,(\omega t) \end{cases} \tag{1}$$

where V_d, V_m and ω are the DC voltage offset, amplitude of the output voltage, and angular frequency, respectively. The DM component is then given by (2), which is the output voltage:

$$v_o = v_A - v_B = V_m\, sin(\omega t) \tag{2}$$

2.1.1 ACTIVE POWER DECOUPLING IN DIFFERENTIAL BUCK INVERTER

Suppose that the inverter topology DBU shown in Fig 2(a) supplies a linear load with a sinusoidal output voltage, given by (2), the instantaneous output power p_o is given by (3).

$$p_o = \frac{V_m I_m}{2}[cos\phi - cos(2\omega t + \phi)] \tag{3}$$

where I_m is the amplitude of the output current and ϕ is the phase angle between the output voltage v_o and the output current i_o. The inherent second-order power component in (3) must be decoupled to prevent it from being transferred to the DC source. As already noted, instead of using a large aluminium capacitor on the DC side, power decoupling in the analyzed topologies is achieved by diverting the power pulsation to a more reliable thin-film capacitor of lower capacity. Neglecting the voltage drop on the output inductors, the power absorbed by the decoupling capacitors must be equal to the power of the oscillating component. This leads to the following first-order differential equation (4),

$$C_1 v_{c1}\frac{dv_{c1}}{dt} + C_2 v_{c2}\frac{dv_{c2}}{dt} = \frac{V_m I_m}{2} cos(2\omega t + \phi) \tag{4}$$

For symmetrical loading of the inverter, it was assumed that ($C_1 = C_2 = C_d$). Knowing the differential output voltage ($v_{C1} - v_{C2}$) given in (2) and solving (4) and (2), the two output voltages result in (5), where S is the apparent power, V_o is the RMS of the output voltage, and K_0 is an initialization parameter, as explained below. Based on the operating constraints of a HB, the voltages across the two decoupling capacitors

must be positive, as shown in (6). Moreover, the part under the square root of (5) must also be positive. These two constraints can be fulfilled by parameter K_0, which can be calculated as in (7).

$$v_{c1,2} = \pm\frac{V_m}{2}\ sin(\omega t) + \frac{1}{2}\sqrt{\frac{2S}{\omega C_d}sin(2\omega t - \phi) - 2V_o^2\ sin^2(\omega t) + \frac{2S}{\omega C_d}sin(\phi)\ + K_0} \tag{5}$$

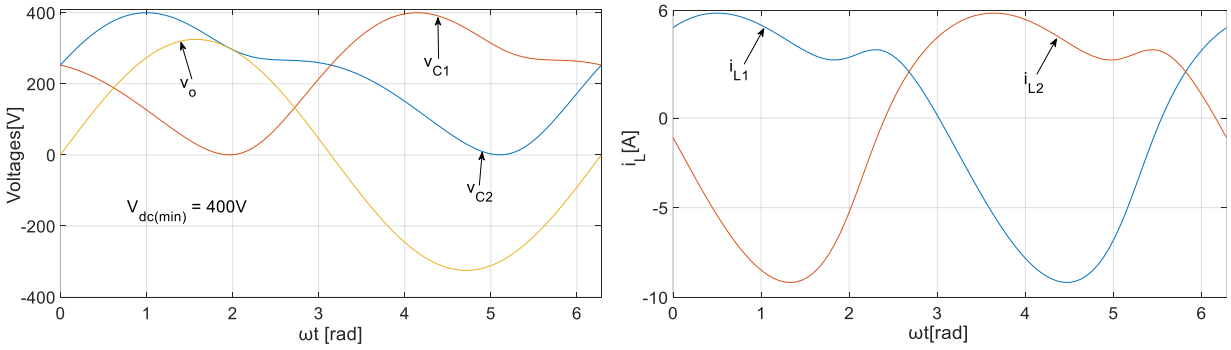
$$v_{c1,2} \geq 0 \quad \forall \omega t \in [0,2\pi] \tag{6}$$

$$K_0 = \max_{0\leq\omega t\leq 2\pi}\left[4V_o^2 sin^2(\omega t) - \frac{2S}{\omega C_d}[sin(2\omega t - \phi) + sin(\phi)\right] \tag{7}$$

If the controller can reshape v_{C1} and v_{C2} to follow (5), APD can be achieved. However, this method is parameter-dependent; hence, precise power decoupling may not be achieved if parameters such as capacitance change, or disturbances exist in the output current. For the main parameters provided in Table 2 and considering resistive load, i.e. $\phi = 0$ (which will be considered the same in the following analysis), Fig 4(a) shows the obtained voltage waveforms v_{C1} and v_{C2} across the decoupling capacitors and the differential output voltage (v_o) under nominal capacitance at rated power. The results show that the maximum voltage of the decoupling capacitance is approximately 1.23 times the maximum value of the output voltage. Hence, the minimum DC input voltage required in this case is greater than that of the conventional H-bridge. Fig 4(b) shows the inverter output current waveforms (i_{L1} and i_{L2}).

Table 2: Inverter main parameters.

Parameter	Value
Output voltage (rms) and frequency	230V, 50Hz
Rated output active power	1 kW
Decoupling capacitance (C_1, C_2)	60 µF



(a) (b)

Fig 4. Differential buck single-phase inverter: (a) voltage waveforms of v_{C1}, v_{C2}, v_O; (b) current waveforms of i_{L1} and i_{L2}.

2.1.2 ACTIVE POWER DECOUPLING IN DIFFERENTIAL BOOST INVERTER

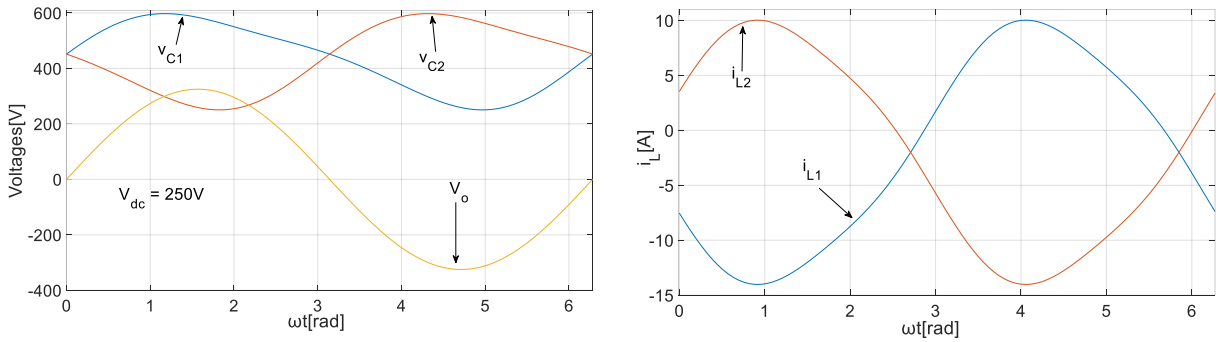
The general topology of a DBO inverter is shown in Fig 2(b). The general equation for v_{C1} and v_{C2} remains the same as that of the DBU topology, as shown in (5), and only K_o is changed to satisfy the new constraint (8) introduced for the DBO inverter.

$$v_{c1,2} \geq V_{dc} \quad \forall \omega t \in [0,2\pi] \tag{8}$$

where V_{dc} denotes the input DC voltage. In this case, K_o is obtained by numerically solving equation (9).

$$K_0 = \max_{0 \leq \omega t \leq 2\pi} \left[4V_{dc}^2 - 4\sqrt{2}V_{dc}V_o \sin(\omega t) + 4V_o^2 \sin^2(\omega t) - \frac{2S}{\omega C_d}[\sin(2\omega t - \phi) + \sin(\phi)] \right] \tag{9}$$

The waveforms of the decoupling capacitances v_{C1} and v_{C2}, and the output differential voltage (v_o), are shown in Fig 5(a). The capacitor voltages are shifted above the DC input voltages. The advantage of this topology is that it can operate with a lower DC input voltage. However, because the voltage across the decoupling capacitors is shifted above the DC input voltage, the decoupling capacitors experience higher voltage stresses. Fig 5(b) shows the inverter current waveforms.



(a) (b)

Fig 5. Differential boost single-phase inverter: (a) voltage waveforms of v_{C1}, v_{C2}, v_O; (b) current waveforms of i_{L1} and i_{L2}.

2.1.3 ACTIVE POWER DECOUPLING IN DIFFERENTIAL BUCK-BOOST INVERTER

The basic structure of DBB is shown in Fig 2(c). It consists of two buck-boost converters (HB-A and HB-B) connected to the same DC input source V_{dc}. The output voltage v_o is the differential voltage across the two decoupling capacitors C_1 and C_2. The DBB can operate in either buck or boost mode depending on the input DC voltage. Similarly, the voltage equations, v_{C1} and v_{C2} remain the same as those of the DBU, as shown in (5). In the buck mode, the value K_o is given by (7), whereas in the boost mode, it is given by (9). Although this topology has a wider operating range for the DC input voltage, the voltage stress across the inverter leg is the highest (sum of the DC input voltage and the voltage across the decoupling capacitor). Fig 6(a) and Fig 6(b) show the waveforms of the decoupling capacitances v_{C1} and v_{C2} for the boost and buck modes, respectively. Fig 6(c) and Fig 6(d) show the output current waveforms for the boost and buck modes, respectively. For practical reasons, a DC voltage of 250V was considered for boost mode [9].

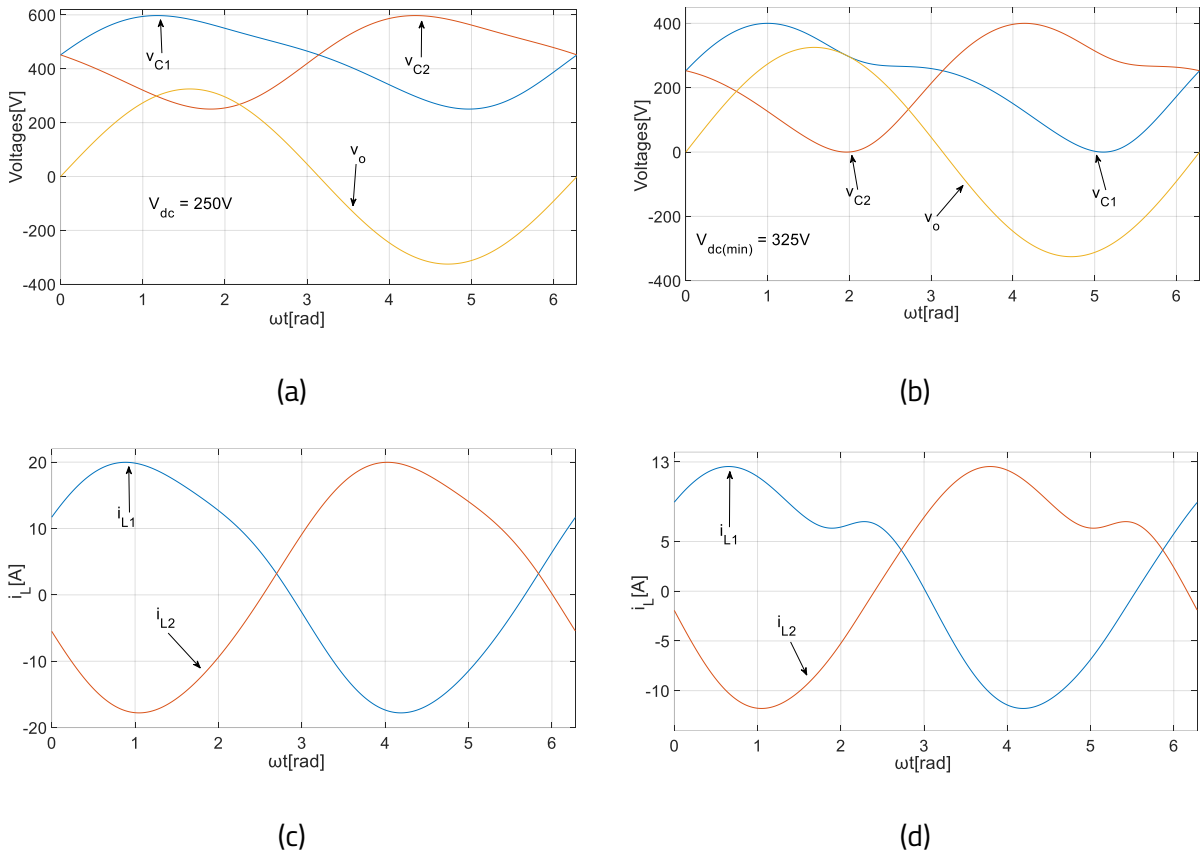


Fig 6. Differential buck-boost single-phase inverter: (a) voltage waveforms of v_{C1}, v_{C2}, v_O in boost mode; (b) voltage waveforms of v_{C1}, v_{C2}, v_O in buck mode; (c) current waveforms of i_{L1} and i_{L2} in boost mode; (d) current waveforms of i_{L1} and i_{L2} in buck mode.

2.1.4 ACTIVE POWER DECOUPLING IN DIFFERENTIAL BUCK INVERTER WITH SPLIT CAPACITOR ON THE AC SIDE

This topology, shown in Fig 3, is derived from DBU [77]. The decoupling capacitors are split into two symmetrical forms. The filtering loop created by the DC source and capacitors C_1, C_3or C_2, C_4 provides a conducting path for high-frequency switching ripples, which reduces the requirements of DC-link capacitors. The oscillating component is processed using all four capacitors, as shown in (10), with constraints (2) and (11).

$$C_1 v_{c1}\frac{dv_{c1}}{dt} + C_2 v_{c2}\frac{dv_{c2}}{dt} + C_3 v_{c3}\frac{dv_{c3}}{dt} + C_4 v_{c4}\frac{dv_{c4}}{dt} = 0.5 V_m I_m \cos(2\omega t + \phi) \tag{10}$$

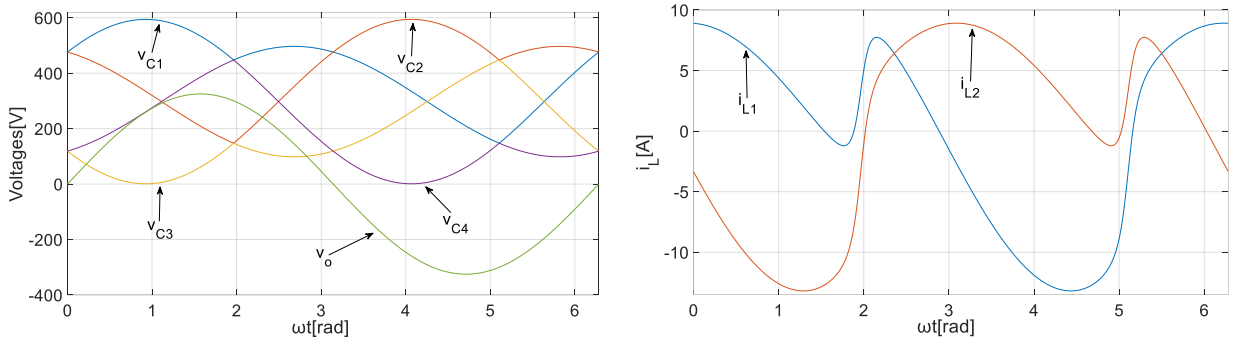
$$\begin{cases} v_{c1,2,3,4} \geq 0 \quad \forall \omega t \in [0, 2\pi] \\ v_{ci} = V_{dc} - v_{c(i-2)} \quad \forall \omega t \in [0, 2\pi] \ \{i = 3,4\} \end{cases} \tag{11}$$

Solving the differential equation (10) with constraints (2) and (11) yields (12), where K_o is obtained by numerically solving the following expression (13).

$$v_{c1,2} = \frac{V_{dc}}{2} \pm \frac{V_m}{2}\ sin(\omega t) + \frac{1}{2}\sqrt{V_{dc}^2 - 2V_o^2\ sin^2(\omega t)\ + \frac{S}{\omega C_d}[sin(2\omega t - \phi)] + sin\ (\phi)] - K_o} \quad (12)$$

$$K_0 = \min_{0 \le \omega t \le 2\pi}\left[V_{dc}^2 - 2V_o^2 sin^2(\omega t) + \frac{S}{\omega C_d}[sin(2\omega t - \phi)] + sin(\phi)\right] \quad (13)$$

The decoupling capacitor waveforms v_{C1}, v_{C2}, v_{C3}, v_{C4} are shown in Fig 7(a), and Fig 7(b) shows the inverter current waveforms.

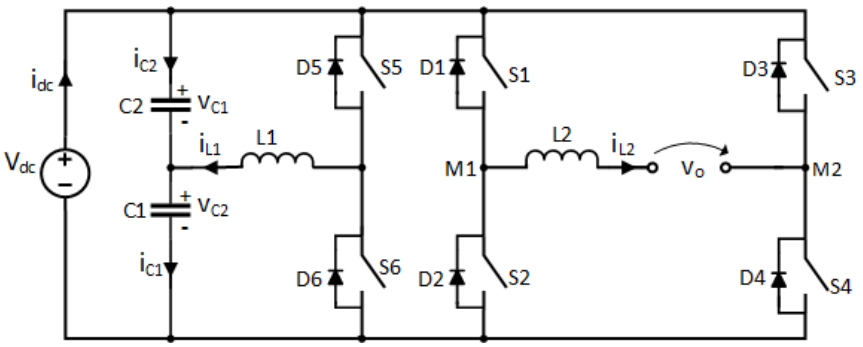


(a) (b)

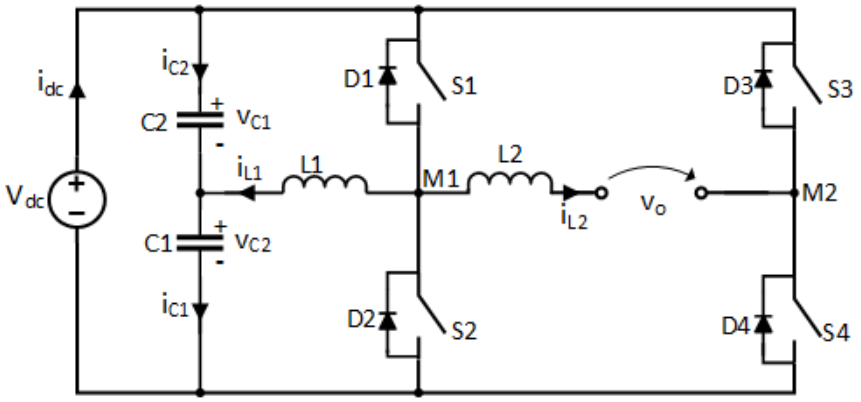
Fig 7. Differential buck inverter with split capacitor on the AC side: (a) voltage waveforms of v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_O ;(b) current waveforms of i_{L1} and i_{L2}.

2.1.5 ACTIVE POWER DECOUPLING FOR H-BRIDGE INVERTER WITH DC SPLIT CAPACITOR AND REDUCED SWITCH COUNT

To provide a balanced analysis of differential single-phase inverters, the H-bridge topology with an additional leg for APD, DSCHB [19], and its derived reduced switch, RS-DSCHB [29], as shown in Fig 8(a) and Fig 8(b,) respectively, were also considered. In Fig 8(a), an additional synchronous buck leg is added to the H-bridge inverter. The DC-link capacitor is also split into two identical capacitors connected in series. The advantage of these topologies is that no additional capacitors are required for the APD, as the same DC-link capacitors will perform the dual functionalities of maintaining a stiff DC-link bus voltage and performing APD.



(a)



(b)

Fig 8. H-Bridge inverter with DC-slit capacitor: (a) H-Bride inverter with synchronous buck active power decoupling; (b) reduced switch count.

The general equation (4) holds for these two topologies with the following constraints:

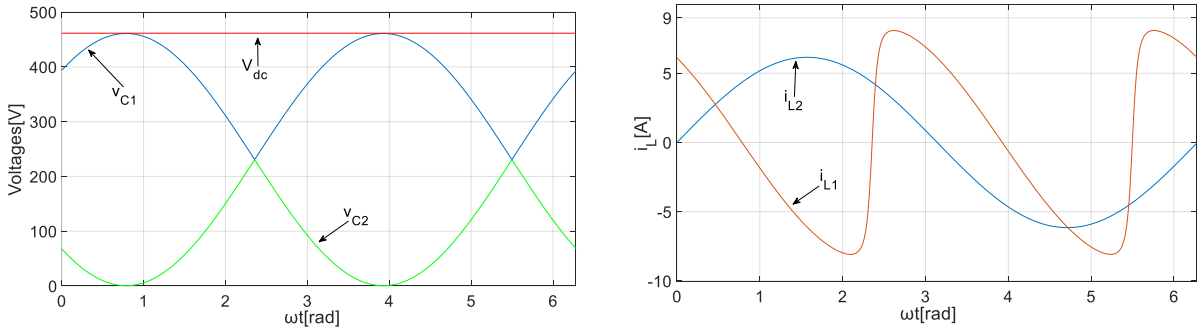
$$\begin{cases} v_{c1,2} \geq 0 \quad \forall\, \omega t \in [0,2\pi] \\ v_o = V_m \sin(\omega t) \\ v_{c2} = V_{dc} - v_{c1} \end{cases} \tag{14}$$

Solving equation (4) with the above-mentioned constraints yields equation (15), where K_o is given by optimization of the function (16).

$$v_{c1} = \frac{V_{dc}}{2} + \frac{1}{2}\sqrt{V_{dc}^2 + \frac{2S}{\omega C_d}[sin(2\omega t - \phi)] + sin\,(\phi) - K_o} \tag{15}$$

$$K_0 = \min_{0 \leq \omega t \leq 2\pi} \left[V_{dc}^2 + \frac{S}{\omega C_d}[sin(2\omega t - \phi)] + sin(\phi) \right] \tag{16}$$

The voltage waveforms of v_{C1} and v_{C2} across the decoupling capacitors for minimum V_{dc} under nominal capacitance and rated power is shown in Fig 9(a) while Fig 9(b)shows the inverter current waveforms.



(a) (b)

Fig 9. H-Bridge inverter with DC-slit capacitor: (a) voltage waveforms of v_{C1}, v_{C2}, v_{dc}; (b) current waveforms of i_{L1} and i_{L2}

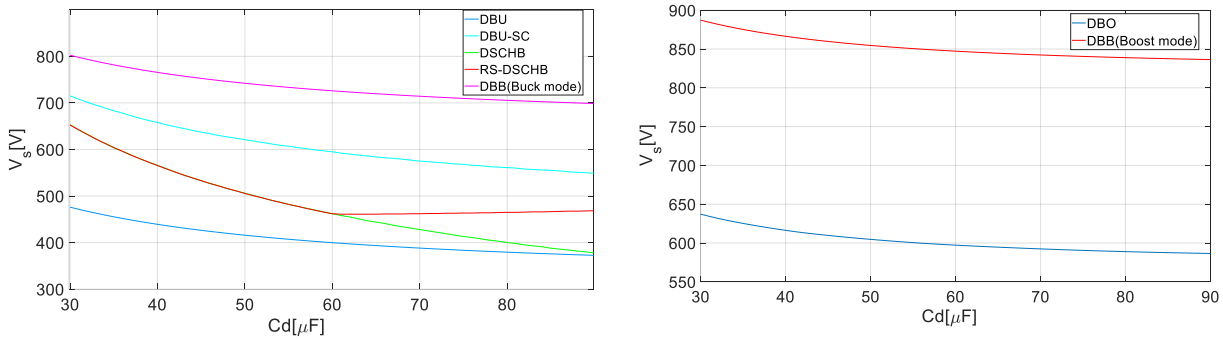
2.2 VOLTAGE STRESS, CURRENT STRESS, AND LOSSES OF APD DIFFERENTIAL INVERTERS

Adding a compensation voltage to achieve APD results in an increase in the voltage stress on the decoupling capacitors and switches, or an increase in the DC-link voltage requirement. The voltage stress on the switch is considered as the voltage across the inverter leg. From the considerations in Table 3, a voltage stress analysis is performed, where V_{cmax} is the maximum voltage on the decoupling capacitors.

Table 3: Voltage limits for switches and decoupling capacitors.

Topology	Voltage stress on the switches	Voltage constraints on the decoupling capacitors
DBU	V_{dc}	$0 \le V_{C1,2} \le V_{dc}$
DBO	V_{cmax}	$V_{C1,2} \ge V_{dc}$
DBB	$V_{dc}+V_{cmax}$	$V_{C1,2} \ge 0$
DBU-SC	V_{dc}	$V_{C1,2,3,4} \ge 0$
DSCHB	V_{dc}	$V_{C1,C2} \ge 0$
RS-DSCHB	V_{dc}	$V_{C1,C2,M1,M2} \ge 0$

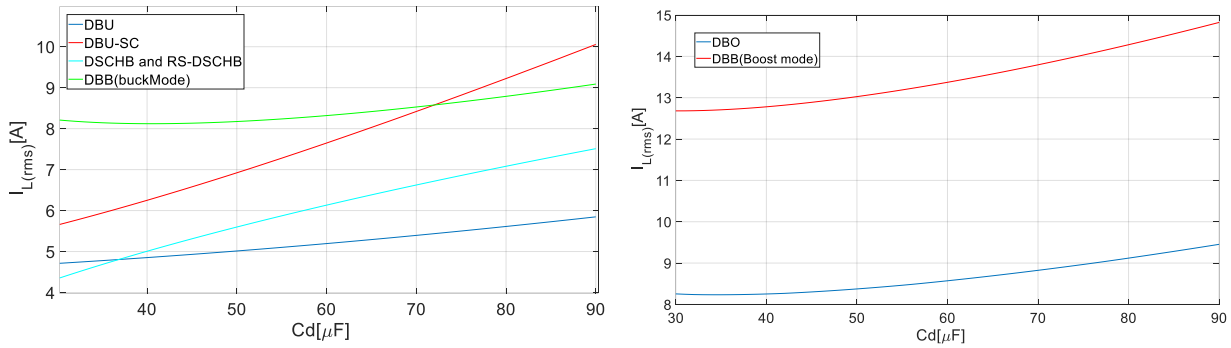
The plot of the minimum voltage stresses on the switches as a function of the decoupling capacitance for the buck and boost topologies is shown in Fig 10(a) and Fig 10(b), respectively. As can be seen, the overall voltage stress on the inverter leg decreased as the capacitance increased. This is because for the same capacitor energy, the voltage of the capacitor is inversely proportional to the square root of the capacitance. Fig 10(a) shows that DBU topology has the lowest switch voltage stress. This makes it possible to use switches with comparatively low voltage ratings, which lower their price. In addition, having a higher safety margin on the switches is beneficial for improving reliability. Moreover, the low-voltage stress on the switches translates to low switching losses, which improves the inverter efficiency and the requirements of the cooling system. In contrast, DBB (in the buck mode) exhibited the highest voltage stress. Among the boost topologies Fig 10(b), DBO has a low voltage stress on switches compared to DBB (in boost mode). Above 60µF it can be noted in Fig 10(a) that the switch voltage stress on DSCHB is lower than that on RS-DSCHB to maintain a voltage v_{M2} positive. The switch stresses of the DBB inverter topology are a combination of the DC link voltage and the stress in the decoupling capacitor, which makes it higher than those of the other topologies.



(a) (b)

Fig 10. Voltage stress: (a)buck topologies; (b) boost topologies.

To analyze the inverter current stresses, the RMS current through the filter inductor was considered, and the plots are shown in Fig 11(a) and Fig 11(b) for the buck and boost topologies, respectively. As shown, the current stress increases as the decoupling capacitance increases. The inverter current stress is important for determining the losses of the switches. Moreover, high current stress implies the need to use filter inductors with a higher saturation current. Therefore, the optimum value of decoupling capacitance should be a compromise between losses and component size. Among the buck topologies, DBU topology also has lower inverter currents, while for boost topologies, the DBO topology has a lower inverter current.



(a) (b)

Fig 11. Current stress: (a) buck topologies; (b) boost topologies.

2.3 SWITCH UTILISATION

As mentioned previously, the minimum number of switches is the main advantage of the analyzed inverter topologies. However, the increase in voltage and current stress implies that the semiconductors are oversized. Often used to analyze converter performance, switch utilization (SU) indicates the ratio between the output power delivered by the converter and the total active switch stress, defined as [84] :

$$SU[\%] = \frac{V_m I_m}{\sum_{k=1}^{n} V_{sk} I_{sk}} \cdot 100 \tag{17}$$

where: V_m, I_m are the inverter peak output voltage and current; V_{sk}, I_{sk} are the maximum voltage and current of the n switches. Table 4 shows the SU of the analyzed inverters, considering the operating conditions corresponding to C_d = 60μF, as discussed previously.

Table 4: SU of the analyzed inverter topologies.

Topology	Conventional	DBU	DBO	DBB (boost mode)	DBB (buck mode)	DBU-SC	DSCHB	RS-DSCHB
SU[%]	25.0	13.6	6.0	3.0	5.5	6.4	9.8	13.6

2.4 LOSS ANALYSIS

Along with minimum complexity, another important feature that must be considered in the analyzed topologies is efficiency. As previously shown, ensuring power decoupling requires an increase in the

voltage and current stress on the transistors, which is expected to lead to increased losses in semiconductors. Therefore, this section analyzes the losses (switching and conduction) of the investigated topologies in comparison with the conventional H-bridge inverter. As single-phase inverters are expected to use wide-bandgap MOSFETs (SiC and GaN) in the future, this analysis focuses on the unique characteristics of these transistors in terms of both conduction and switching losses. Additionally, for the purpose of simplification and generalization, the conduction and switching losses are analyzed separately and normalized considering as base values the conduction and switching losses of a conventional H-bridge inverter that uses the same MOSFET type and operates under similar conditions. The voltages and currents previously determined for each topology were considered in the calculation of conduction and switching losses. Considering the same capacitance for the decoupling capacitors (C_d = 60μF), Table 5 presents the optimum (theoretical) voltage of the DC source (V_{dc}) of each topology to produce the rated output AC voltage mentioned in Table 2, and the DC-link voltage of the HB (which may be the same as V_{dc} or different, depending on topology), both provided in per unit (p.u.) considering the magnitude of the AC voltage (V_m) as the base value.

Table 5: Optimum voltages (dc source and half bridge).

Topology	DC Source (V_{dc}) (p.u.)	Half bridge DC-link voltage (p.u.)
Conventional	1.00	1.00
DBU	1.23	1.23
DBO	0.77	0.77 – 1.84
DBB (buck mode)	1.00	1.00 – 2.23
DBB (boost mode)	0.77	1.54 – 2.61
DBU-SC	1.83	1.83
DSCHB	1.42	1.42
RS-DSCHB	1.42	1.42

As previously mentioned, considering the implementation with MOSFETs, the normalized conduction losses to the conduction losses of the conventional inverter are estimated using the following equation:

$$\frac{P_c}{P_{c-conv}} = \left(\frac{I_{rms}}{I_{rms-conv}}\right)^2 \tag{18}$$

where: I_{rms} and $I_{rms\text{-}conv}$ are the RMS currents of the analyzed topology and conventional inverter, respectively. In the above equation, it was assumed that the MOSFET on-state resistances in the 1st and 3rd quadrants (i.e., for the direct and reverse current paths) are the same, while the conduction losses occurring in the body diodes during dead time are neglected (i.e., dead time was considered less than 1% of the switching time). In the analysis of switching loss analysis, it was assumed that the switching frequency is constant for all topologies, whereas the total switching energy of the MOSFET was considered directly proportional to the voltage and current handled by the transistor at the switching instant [85]. Moreover, no switching losses occur in the SiC/GaN body diode. Therefore, the normalized switching losses relative to the switching losses of the conventional inverter are estimated as follows:

$$\frac{P_{sw}}{P_{sw-conv}} = \frac{1}{n}\sum_{k=1}^{n}\left(\frac{V_s(k)}{V_{s-conv}(k)} \cdot \frac{I_s(k)}{I_{s-conv}(k)}\right) \tag{19}$$

where: V_s, $V_{s\text{-}conv}$, I_s, $I_{s\text{-}conv}$ are the voltages and currents of the analyzed topology and conventional inverter, respectively, at switching instant k, and n is the total number of commutations during one period of the output voltage.

Based on the above calculation procedure, the conduction and switching losses for the analyzed topologies are listed in Table 6. Note that the two loss components are normalized to different factors; therefore, their summation does not reflect a value corresponding to the total losses. As shown, the DBU has the smallest losses, whereas the RS-DSCHB topology follows closely. As expected, DBB is the topology with the highest losses as it is configured to accept a wider input voltage variation at the expense of lower switch utilization

Table 6: Analysis of conduction and switching losses.

Topology	Conduction Losses (p.u.) $\frac{P_c}{P_{c-conv}}$	Switching Losses (p.u.) $\frac{P_{sw}}{P_{sw-conv}}$
Conventional	1	1
DBU	1.43	1.46
DBO	3.89	2.78
DBB (buck mode)	3.66	3.34
DBB (boost mode)	9.4	6.63
DBU-SC	3.10	3.10
DSCHB	1.99	2.41
RS-DSCHB	1.49	1.71

As the above analysis was based on a simplified calculation procedure, the conventional and DBU topologies were further investigated using computer simulations and experiments based on the procedure described in [65]. The main parameters used in both the simulation and the experiment are listed in Table 7. It should be noted that the SiC inverter used in the experimental analysis presented in this section is part of the setup described in Chapter 6, Fig 32.

Table 7: Main inverter (SiC) parameters used in simulation and experiment.

Parameter description	Conventional H-bridge inverter	DBU inverter
Rated output active power	1kW	
DC input voltage	450V	
Output RMS voltage	230V	
Filter Capacitor	4.4μF	-
Power decoupling capacitors	-	$C_1 = C_2 = 60\mu F$
Switching frequency	50 kHz	
Filter Inductors	L1 = L2 = 280μH	
MOSFETs type (SiC)	C3M0120090J	

In the experiment, the total losses of the SiC inverter were measured using a precise power analyzer (Yokogawa WT-1806). Table 8 provides a comparison of the simulation and experimental results for losses in both topologies. It should be noted that while in the simulation, the various loss components (i.e., switching and conduction losses of semiconductors, snubbers, inductors, and capacitors) can be estimated, in the experimental analysis, only the overall inverter losses could be measured. The results show that the total losses in the simulation are close to the experimental ones, indicating that the simulation model is accurate enough to be used as a reference and to compare the conduction and switching losses from the simulation with the previously calculated values.

Table 8: Comparative analysis of inverter losses (simulation and experiment).

Topology	Losses (simulation) [W]					Total losses (exp) [W]
	Cond.	Sw.	Cond.+Sw.	Misc.*	Total	
Conv.	8.39	3.04	11.43	11.03	22.46	24.08
DBU	11.44	3.2	14.64	12.79	27.43	29.28

**Additional losses occurring in snubbers, output inductors, decoupling capacitors.*

Table 9 displays the conduction and switching losses of the DBU inverter, normalized to the losses of the conventional inverter, obtained from the simulations and calculations.

Table 9: DBU inverter normalized losses (simulation and calculation).

	DBU Conduction Losses (p.u.) $\frac{P_c}{P_{c-conv}}$	DBU Switching Losses (p.u.) $\frac{P_{sw}}{P_{sw-conv}}$
Simulation	1.36	1.05
Calculation	1.43	1.19

2.5 CONCLUSION

This chapter presented single-phase differential topologies that have been implemented in the literature to achieve APD. Allowing APD without increasing the hardware complexity of the inverter, that is, no extra semiconductor devices are required, poses a considerable practical interest in terms of lowering cost and improving reliability. Therefore, the current study analyzed various differential inverters proposed in the literature (divided into three main classes: buck, boost, and buck-boost) in terms of switch voltage and current stresses, switch utilization, and losses. A unified mathematical description of each topology was also provided, allowing an easier evaluation of the inverters' operational limits under different parameters. Furthermore, the most common control strategies were discussed, and the main idea was to autonomously generate the compensation voltage for the effective decoupling of the oscillating power component. This minimizes the dependency of the control method on the system parameters.

3. CONTROL OF A SINGLE-PHASE DIFFERENTIAL INVERTER AND ITS INTEGRATION WITH ADVANCED CONTROL BASED ON VAN DER POL VOC FOR MG INTEGRATION

Contents of this section has been published by the author in the proceedings 2024 6th Global Power, Energy and Communication Conferences(GPECOM) [86] *and 2025,14th international conference on renewable energy research and applications* [87].

VOC has emerged as an alternative solution for controlling parallel connected inverters in MGs due to its self-synchronization and advanced control capabilities. Compared to droop control and VSM whose operations are derived from the operation of conventional generators, VOC is based on the dynamics of non-linear oscillators such as dead-zone, Van der Pol and Andronov- Hopf oscillators (AHO), which inherently provide synchronism when coupled within a network. Weakly non-linear oscillators synchronize to a steady-state sinusoidal limit cycle from an arbitrary initial condition. However, despite being non-linear, it was shown in [88], [89] that VOC subsumes droop in the steady-state, but is superior in the transient regime due to its faster synchronization speed.

Numerous research efforts have been devoted to exploring VOC, motivated by its significant potential to enhance MG performance through decentralized synchronization and fast dynamic response. A comparison between droop control and VOC is provided in [90], where it was shown that VOC provides relatively faster and damped response. To achieve power synchronism, droop control operates on phasor quantities, i.e. active and reactive powers, and the use of low-pass filters on the power loops impacts its dynamic performance. The challenge with the Van der Pol oscillator is the presence of the third harmonic due to the non-linear voltage dependent current source.

3.1 VIRTUAL OSCILLATOR CONTROL

VOC emulates the dynamics of a non-linear oscillator such as Van der Pol oscillator. Fig 12(a) shows a typical model of a Van der Pol oscillator, where i_{VOC} is the sensed feedback current from the inverter and v_{ref} is the reference voltage from the oscillator. The structure is composed of a resonant tank LC circuit that establishes the system frequency, a non-linear voltage-dependent current source, and a damping resistance. The VOC dynamics are given by the following equations [25]:

$$L\frac{di_L}{dt} = \frac{v_{ref}}{k_v} \tag{20}$$

$$C\frac{dv_{ref}}{dt} = -\alpha\frac{v_{ref}^3}{k_v^2} + \sigma v_{ref} - k_v i_L - k_v k_i i_o \tag{21}$$

where L and C are the virtual inductance and capacitance respectively.

The parameters α and σ are the voltage regulation parameters. The interface between the VOC and the inverter is achieved through the current gain k_i and the voltage gain k_v. The gain k_i operates on the inverter output current before being fed to the VOC while k_v operates the output voltage from the VOC to generate the reference voltage v_{ref} for modulating the inverter. The reference voltage for the inverter is generated as follows:

$$v_{ref} = k_v(v_{voc}cos\phi - \varepsilon i_L sin\phi) \tag{22}$$

where ε denotes the characteristic impedance given as follows, $\varepsilon = (L/C)$.

Depending on the droop characteristics, Φ can be chosen to be zero as in the conventional VOC, producing a relationship between active power(P)- voltage(V) and reactive power (Q) - frequency(ω) or 90 degrees as in inverse VOC. Inverse VOC produces a steady state droop relationship between P - ω and $Q - V$, compatible with the droop characteristics in synchronous machines.

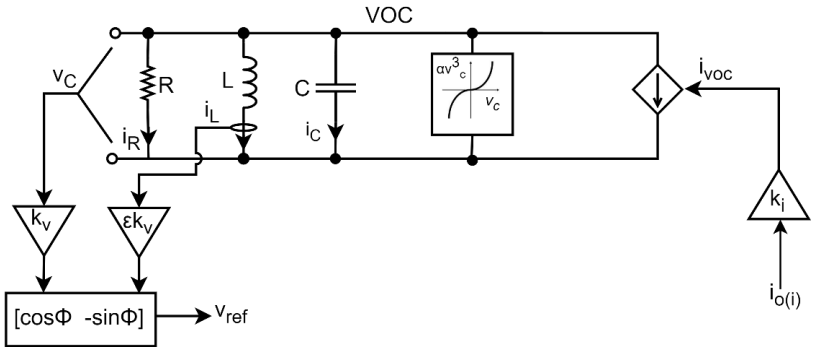


Fig 12. VOC based on Van der Pol oscillator

Fig 13 shows the overall control structure for generating the inverter PWM pulses. The controller is composed of a VOC which generates the reference voltage for inner voltage and current control loops. In addition, an APD controller generates a CM mode component that is added to the modulating signals. The resonant controller was tuned to achieve high gains at even multiples of the fundamental frequency i.e. 2^{nd}, 4^{th} and 6^{th} order harmonics present in the DC-link voltage. The APD controller produces a compensation voltage v_{comp}, which is added to the inverter modulation voltages to generate the pulses for the two legs. The output voltage, which is a differential component, will not be influenced by this CM component. The dynamic of the APD controller is given by the transfer function below:

$$G_d(s) = \frac{v_{comp}}{V_{dc}} = \sum_{j=2,4,6} \frac{2k_{jD}\omega_j}{s^2 + \omega_j^2} \tag{23}$$

where k_{jD} is the gain of the corresponding j_{th} component and ω_j is the fundamental angular frequency.

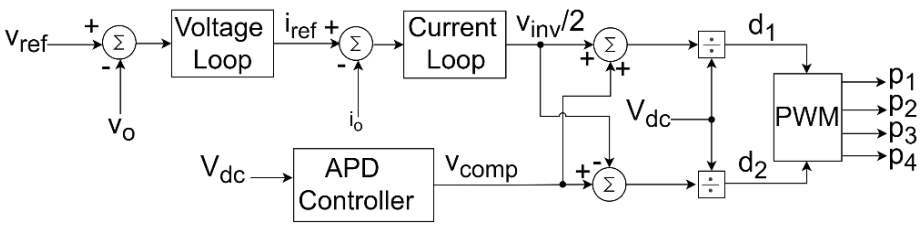


Fig 13. Inverter control structure with VOC and APD

3.2 PROPOSED VOC-BASED STRUCTURE OF THE DBU SINGLE-PHASE INVERTER

The inverter terminal voltage is controlled by the VOC programmed into the digital controller as shown in Fig 14. An additional APD controller is also included to remove the low frequency oscillations in the DC-link, as detailed in section 3.2. The processing of these oscillations is done by the decoupling

capacitors C_1 and C_2 of the DBU inverter shown in Fig 14. Through APD control, the oscillations are redirected to the capacitors C_1 and C_2.

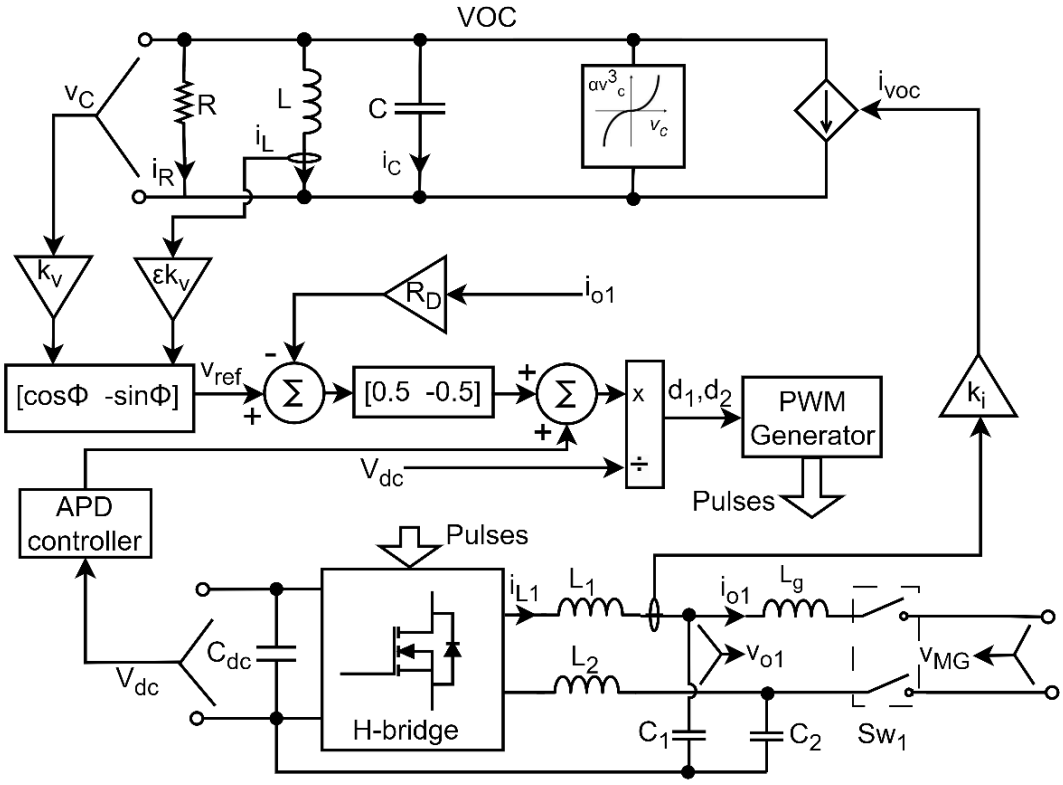


Fig 14. Proposed control structure on a DBU inverter.

3.3 EXPERIMENTAL RESULTS ON CONVENTIONAL VOC

To assess the performance of the system both in steady-state and under disturbances, an experimental setup was implemented as detailed in Chapter 6, laboratory setup 1. The setup comprises a real-time controller for rapid control prototyping (RCP), dSPACE DS1103. Two SiC MOSFET high switching evaluation boards make up the inverter hardware. The input voltage of 450V was provided by a DC power supply. Measurements were performed in the Control Desk software environment. The main parameters used in the experiment are shown in Table 12 in next Chapter.

3.3.1 DYNAMIC RESPONSE

Fig 15 and Fig 16 show the dynamic response of the inverter when linear load is switched on and off. The figures show the main waveforms that include the inverter output currents, output voltage, duty cycles, DC-link voltage and active power. In both scenarios the system remains stable, and the DC-link voltage is confined within the limits being able to stabilize with approximately 60ms, showing the good performance of the control algorithms as well as its adaptability to applications where the load changes quickly.

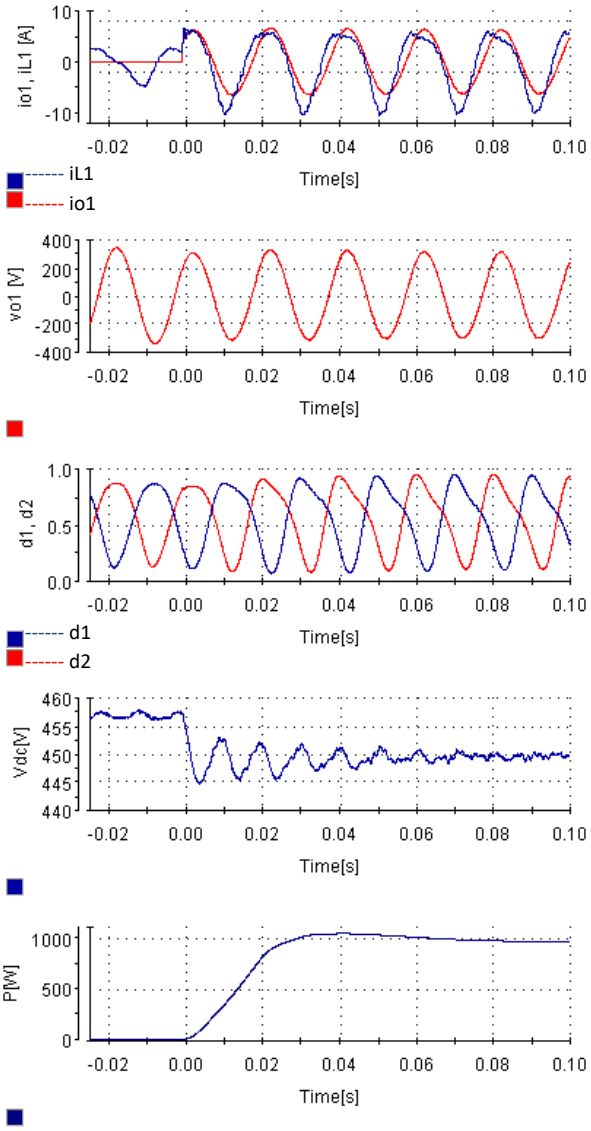


Fig 15. Switching on linear load: output current; output voltage; duty cycles; DC-link voltage; active power.

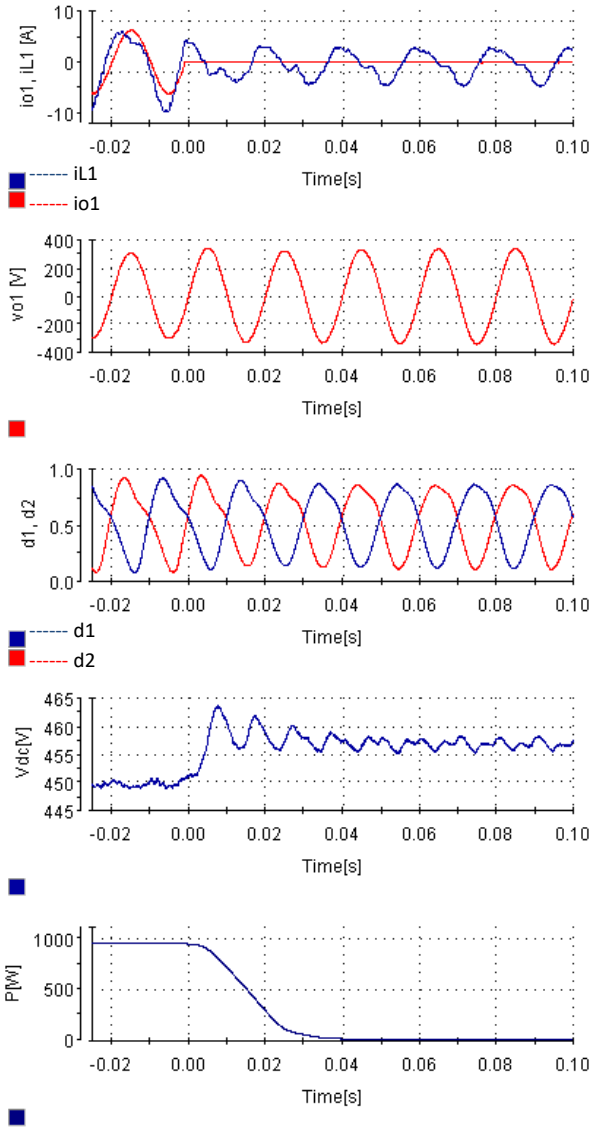


Fig 16. Switching off linear load: output current; output voltage; duty cycles; DC-link voltage; active power.

3.4 EXPERIMENTAL RESULTS OF INVERSE VOC ON A SINGLE-PHASE INVERTER

In this section, the experimental results of inverse VOC are presented. Inverse VOC are studied because its P - ω and Q – V relationships are naturally compatible with synchronous machines, ensuring proportional power sharing and stable operation when inverters operate alongside conventional generators. Section 3.1 details how the oscillator generates the reference voltage to achieve the inverse relationship.

3.4.1 DYNAMIC RESPONSE WITH LINEAR LOAD

The dynamic response was analyzed by subjecting the system to a step change in load (switching on or off 1kW linear load). Fig 17 and Fig 18 show the main waveforms for the two cases (switching on or switching off a linear load), that include the inverter output current (filter inductor and output), output voltage, duty cycles, DC-link voltage and active power. In both scenarios, i.e. switching on or off the

load, the inverter was able to provide responsiveness regulating the output voltage and stabilizing the DC-link voltage in about 3 cycles. This is critical in real-world applications where good steady-state and dynamic performance are required.

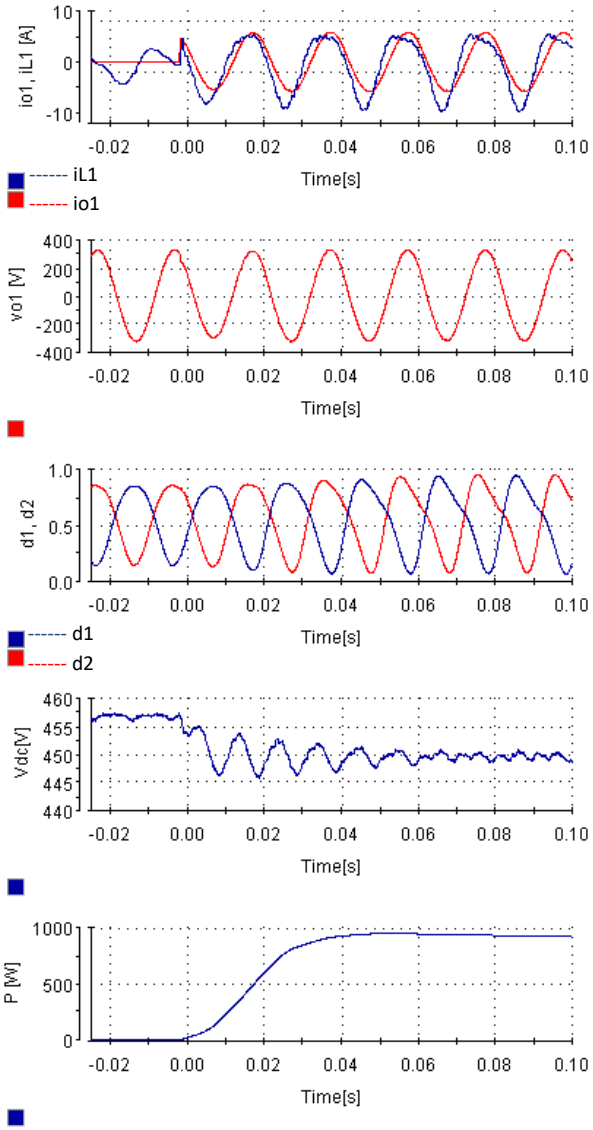


Fig 17. Switching on linear load: output current; output voltage; duty cycles; DC-link voltage; active power.

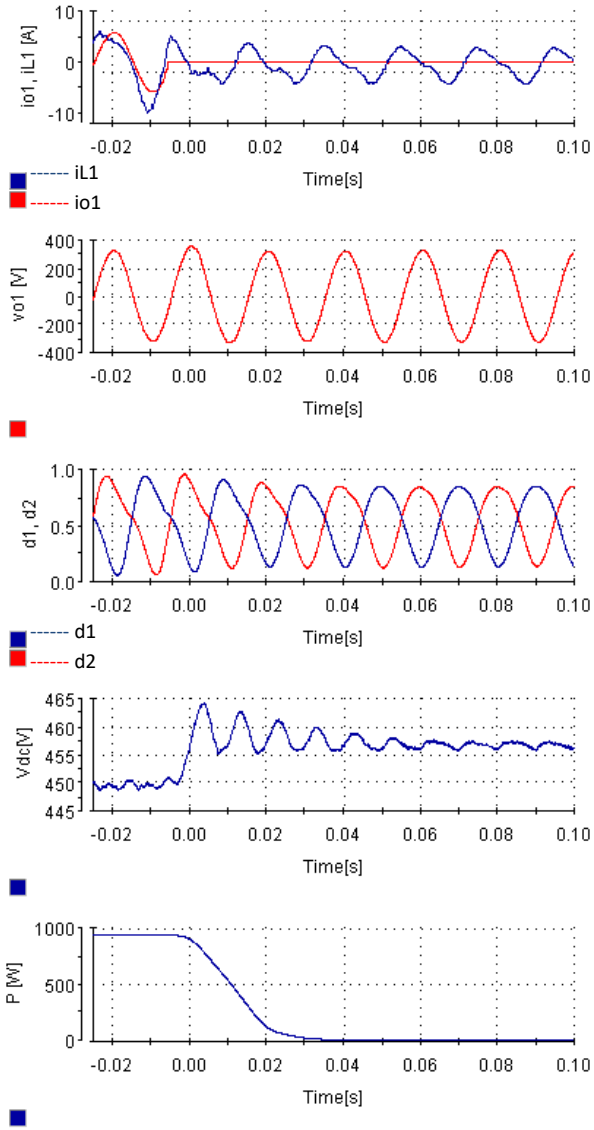


Fig 18. Switching off linear load: output current; output voltage; duty cycles; DC-link voltage; active power.

3.4.2 COMPARATIVE ANALYSIS BETWEEN CONVENTIONAL AND INVERSE VOC

In this section, a comparative assessment between the inverse and conventional VOC was done based on the THD of the output voltage of DBU inverter and conventional single-phase inverter. In the analysis, an output filter capacitor of 10µF and a DC-link capacitance of 1000µF was considered in the case of conventional single-phase inverter. All the other parameters were the same as those shown in Table 12. Table 10 and Table 11 shows the THD of the output voltage for DBU inverter with APD and the conventional single-phase inverter respectively. For the cases considered, inverse VOC achieved low THD compared to the conventional VOC at nominal voltage and frequency under different loading conditions. The system was restored to nominal voltage and frequency by tuning the oscillator parameters α and C, respectively. The low THD can be attributed to the harmonic current filtering of

the VOC virtual inductor, thus using virtual inductor current as the reference from the VOC results in low THD of the output voltage. Additionally, small difference between the THD of the DBU inverter with APD and the conventional single-phase inverter for both control algorithms, demonstrates that APD does not affect the THD of the output voltage.

Table 10: Total harmonic distortion of load voltage in DBU Inverter.

	THD_V [%]	
Parameter	Inverse VOC	Conventional VOC
P = 0kW, Q = 0kVAr	0.75	2.46
P = 0kW, Q= 1kVAr (capacitive)	0.93	2.98
P = 0kW, Q = 1kVAr (inductive)	0.89	2.38
P = 1kW, Q = 0kVAr	0.82	2.26
P = 0.8kW, Q =0.6kVAr (inductive)	0.81	2.22
P =0.8kW, Q =0.6kVAr (capacitive)	0.78	2.35
Non-linear load, (0.5kW/1kVA)	3.8	4.10

Table 11: Total harmonic distortion of load voltage in conventional single-phase Inverter.

	THD_V [%]	
Parameter	Inverse VOC	Conventional VOC
P = 0kW, Q = 0kVAr	0.81	2.4
P = 0kW, Q= 1kVAr (capacitive)	1.04	2.81
P = 0kW, Q = 1kVAr (inductive)	0.74	2.36
P = 1kW, Q = 0kVAr	0.82	2.19
P = 0.8kW, Q =0.6kVAr (inductive)	0.77	2.19
P =0.8kW, Q =0.6kVAr (capacitive)	0.87	2.25
Non-linear load, (0.5kW/1kVA)	4.62	4.92

3.5 CONCLUSION

This chapter has presented the development and analysis of VOC scheme formulated from the Van der Pol nonlinear oscillator. Starting from its structure and operating principles, the chapter established an understanding of how VOC regulates inverter terminal and frequency. Both the conventional and inverse VOC architectures were examined, and their steady-state and dynamic behaviors were analyzed on a single-phase inverter. Inverse VOC provides a link between P - ω and Q – V. This relationship is compatible with the natural dynamics of synchronous machines. Compared to the conventional VOC, inverse VOC showed lower output voltage THD at nominal voltage and frequency for different loading conditions. APD was also integrated with VOC, and the stablished control was effective in eliminating the low frequency oscillations inherent in the DC-link. The analysis was done under both linear and nonlinear loading conditions to provide an understanding of how the proposed control performs in environments with load-induced distortions. During the transitory regimes induced by switching the full non-linear load on and off, the DC-link voltage was restored within less than 20ms.

Based on the analysis presented in this Chapter, the next chapters will further explore the use of VOC for controlling parallel inverters in an MG.

4. CONTROL OF SINGLE-PHASE ISLANDED MICROGRID BASED ON VAN DER POL VOC ENHANCED WITH POWER LIMITATION AND ROBUST DISTRIBUTED SECONDARY CONTROL

The contents of this chapter has been published by the author in IEEE open Journal of the Industrial Electronics Society, Volume 6, 2025 [91] *.*

The global energy landscape is undergoing a major paradigm shift from traditional synchronous machine-dominated power systems to converter-dominated power systems [92]. The shift to inverter-based resources such as PV, wind, and batteries is largely influenced by the need to adopt sustainable clean energy to meet increasing energy needs. The transition to a more resilient and decentralized power system can be facilitated by MGs [93], [94]. MGs aggregate various DERs and load into a controllable unit, capable of operating either standalone or connected to another grid. Several key benefits can be derived from MGs, including improved energy security, reliability, sustainability, and reducing carbon emissions [95]. At the same time, stability challenges are more acute in MGs because of the weak nature of these systems [96]. As a result, more research should be directed primarily towards developing control algorithms that ensure stable and efficient coordinated operation of various DERs.

Currently, a large percentage of inverter-based resources are controlled through a GFL converter [97], which works well when connected to a stiff grid. The GFL controller controls the inverter to behave as a current source in the sub-transient time frame. During operation, the inverter must maintain synchronization with the grid through a phase-locked loop (PLL). The need for a voltage source to synchronize with poses challenges for GFL controllers, particularly in weak grids, or during system splits. Furthermore, these GFL inverters are unable to participate in processes such as black start in the event of a total or partial grid shutdown.

As the landscape transitions towards more decentralized energy generation, GFM control has emerged as a key enabling technology to overcome the challenges mentioned above [98]. The GFM controller controls the inverter to behave as a voltage source in the sub-transient time frame, and it autonomously establishes the inverter's internal voltage and phase angle. GFM controller uses power/ current based synchronization and tends to be relatively stable in weak grids due to its non-reliance on PLL to remain synchronized with the rest of the network. Adopting GFM control enhances the stability and reliability of the MG [99]. In addition, GFM can provide other ancillary services, such as black start capability.

4.1 SYSTEM STRUCTURE

Fig 19 shows the structure of the considered islanded MG consisting of three parallel single-phase inverters. Each inverter is connected to the PCC through a switch (Sw_i). The series impedance is mainly provided by the inductors L_1, L_2, and L_3(and their corresponding resistances), which ensure higher order harmonic filtering as well as acting as coupling inductors.

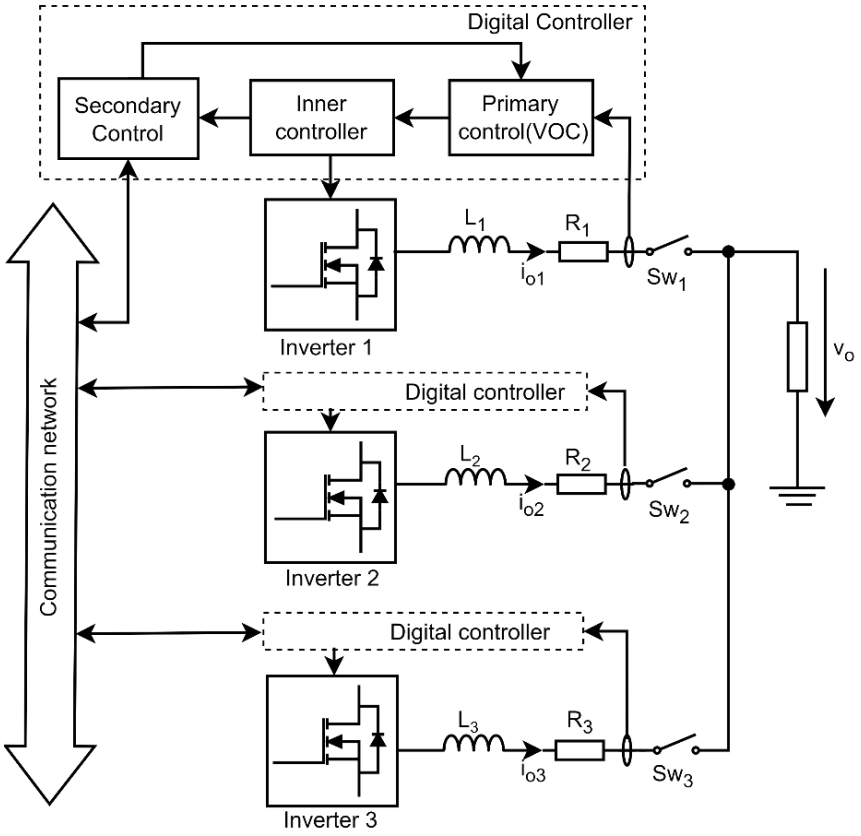


Fig 19. The structure of the proposed MG consisting of three parallel inverters.

4.2 CONTROL OF THE PROPOSED MICROGRID

Fig 20 shows the overall control structure of one inverter (the others having a similar control), composed of the implemented primary and secondary control layers. The following sections detail each subsystem of the proposed control.

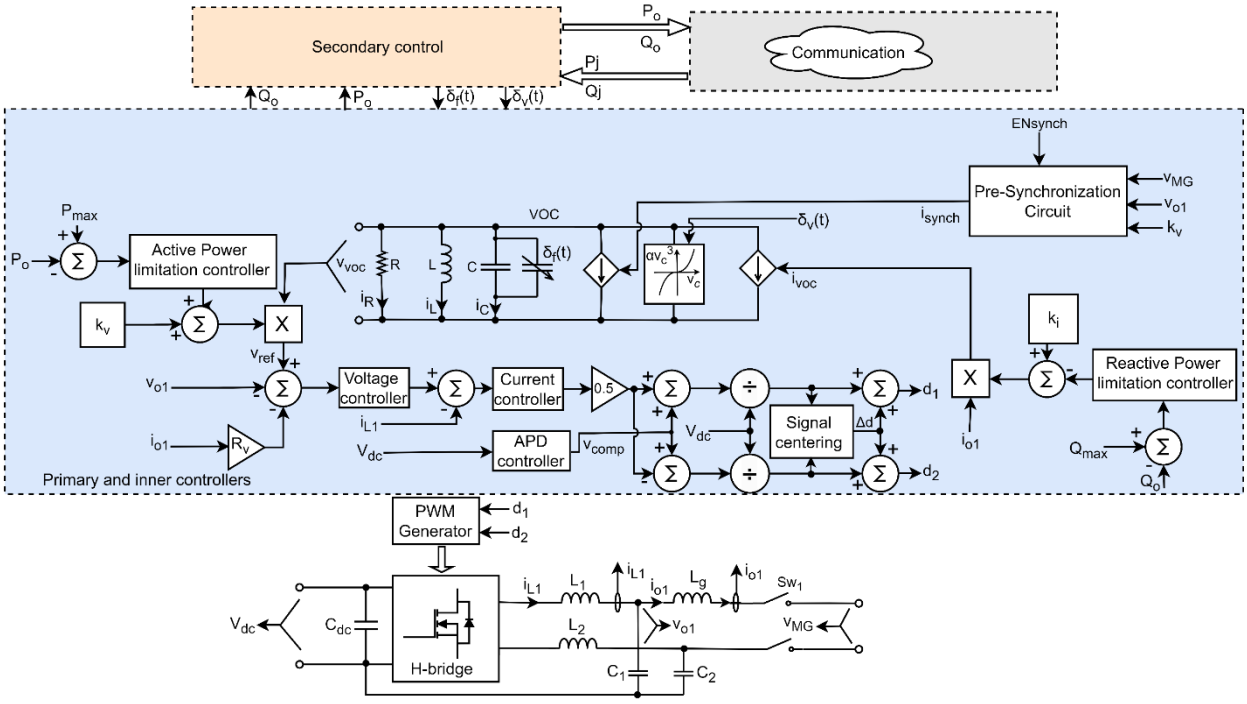


Fig 20. Overall control structure of one inverter with primary and secondary control loops.

4.2.1 SECONDARY CONTROL

The proposed secondary controller described by (24) and (25) uses local information and collects data from its immediate neighbors to improve the global optimization performance of the whole MG system and control actions coordination. Through this control, the effects of clock drift on the secondary control are mitigated, as clearly evidenced by experimental measurements. The first term of the proposed secondary frequency controller compares the measured frequency at the PCC to the nominal frequency and the error passed through an integrator. The secondary voltage controller compares the nominal RMS voltage to the average of the RMS voltages of all inverters. Through this way, the average voltage of all nodes is brought closer to the nominal voltage. This approach helps to solve the conflict between voltage regulation and active power sharing. The second term is generated by each inverter through comparing its normalized power to the average normalized powers of its nearest neighbors. The error generated is also passed through the integrator, and the two terms are combined to generate compensatory terms. In this way, both frequency and voltage regulation and power sharing are achieved. The averaging of voltages and powers in (24) and (25) occur each time a new packet containing data from a neighbor inverter arrives through the communication channel. For frequency restoration, the generated compensatory term is added to the virtual capacitance of the VOC as follows: $C_{new} = C + \delta_f(t)$, where C is the nominal capacitance. In the case of voltage, the generated compensatory term is added to the VOC alpha term as follows: $\alpha_{new} = \alpha + \delta_v(t)$. The secondary controllers are described by (24) and (25).

$$\delta_f(t) = k_{If} \int (\omega_0 - \omega_i)dt + k_{IQ} \int \left(\frac{Q_i}{Q_i^*} - \frac{1}{n} \sum_{j=1}^{n} \frac{Q_j}{Q_j^*} \right) dt \tag{24}$$

$$\delta_{V(i)}(t) = k_{IV} \int \left(V_0 - \frac{1}{n+1} \left(V_i + \sum_{j=1}^{n} V_j \right) \right) dt - k_{IP} \int \left(\frac{P_i}{P_i^*} - \frac{1}{n} \sum_{j=1}^{n} \frac{P_j}{P_j^*} \right) dt \tag{25}$$

where k_{If}, k_{IV}, k_{IQ} and k_{IP} are the integrator gains. P^*_i and Q^*_i are the rated active and reactive power of the current inverter while P^*_j and Q^*_j are the rated active and reactive power of the neighboring inverters.

4.3 EXPERIMENTAL VALIDATION

To validate the simulation results, an experimental setup was built as shown in chapter 6, setup 1, according to the MG structure presented in Fig. 2, with the MG setup consisting of two inverters. Each inverter was controlled by a separate dSPACE DS1103 controller, and the waveforms were acquired through ControlDesk software. Control of the inverters followed RCP. Secondary control communication was achieved through CAN protocol. In this setup two separate DC sources were used. Detailed information about the setup is provided in Chapter 6. The parameters of system are synthesized in Table 12. The analysis presented below synthesizes different case scenarios to experimentally validate the operation of the proposed system.

Table 12: System parameters.

Symbol	Quantity	Value
S	output apparent power	1 kVA
V_o	rated output voltage	230 V
f	rated output frequency	50 Hz
f_s	switching frequency	40 kHz
V_{dc}	DC-link voltage	450 V
C_{d1}, C_{d2}	decoupling capacitors	60 µF
L_1, L_2	filter inductances	280µH
L_g	grid side inductance	2.5mH

4.3.1 SECONDARY CONTROL

To demonstrate the effect of clock drift on the performance of the secondary controller, a decentralized secondary control was implemented with only local integrators and no communication between the inverters. The results are shown in Fig 21. The secondary control was enabled at t = 6s. Despite the controller being able to regulate the frequency and voltage to their nominal values, it can be observed that the active powers continue to diverge as time progresses because of clock drift, resulting in an unstable equilibrium operating condition.

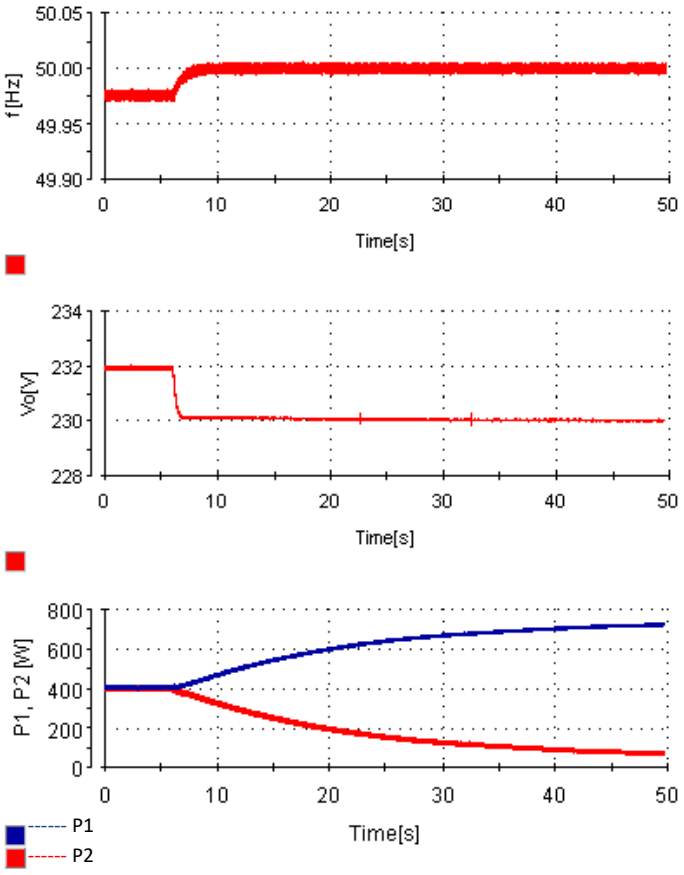
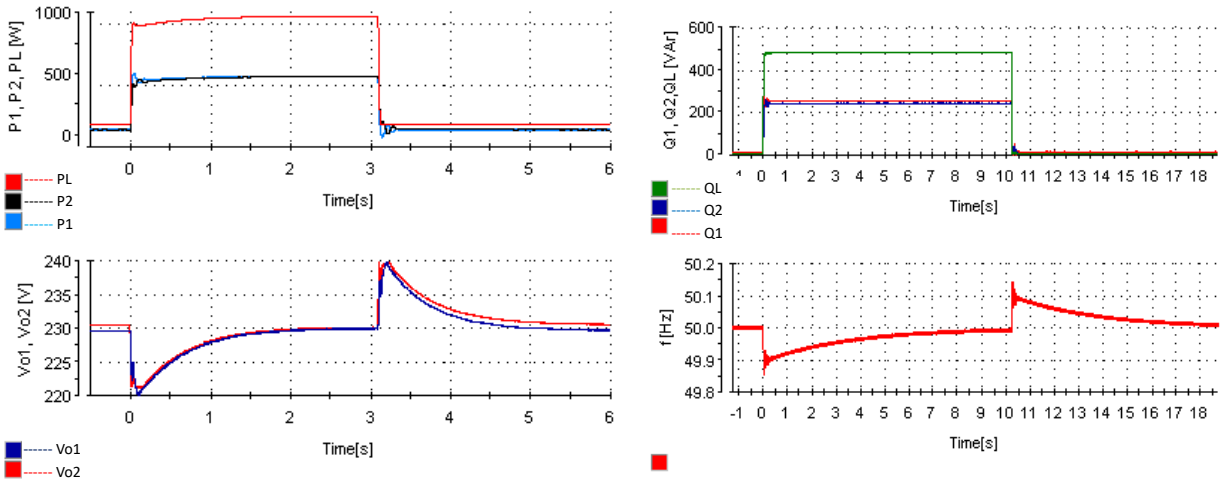


Fig 21. Secondary control with local integrators.

With the implementation of the proposed secondary control method, where each inverter exchanges information about the active and reactive powers, the challenges introduced by the clock drift are

curtailed. Furthermore, the proposed secondary control maintains power sharing, ensuring proportional power contribution from each inverter and preventing excessive strain on any unit.



(a) (b)

Fig 22. Secondary control with the proposed control: (a) step change in active power; (b) step change in reactive power.

To evaluate the accuracy of the active and reactive power sharing of each unit, the power sharing error of the i_{th} unit can be defined as (26) and (27).

$$P_{err(i)\,\%} = \left|\frac{P_{(i,ref)} - P_i}{P_{(i,ref)}}\right| . 100 \tag{26}$$

$$Q_{err(i)\,\%} = \left|\frac{Q_{(i,ref)} - Q_i}{Q_{(i,ref)}}\right| . 100 \tag{27}$$

where $P_{(i,ref}$ and $Q_{(i,ref)}$ are the reference active and reactive power respectively. P_i and Q_i are the actual inverter output powers of the i_{th} unit.

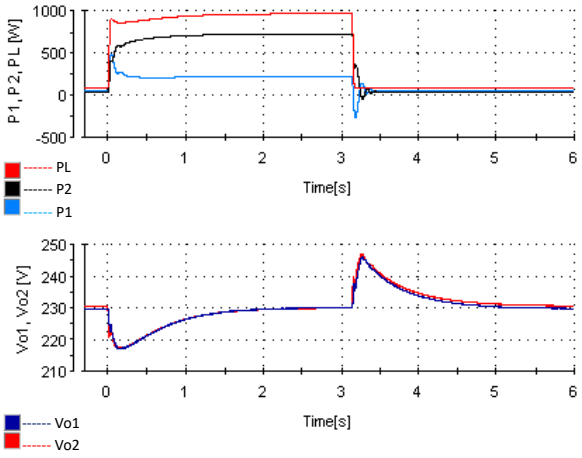
As shown in Fig 21, P_1 and P_2 diverge with time. Fig 22(a) shows the performance of the proposed secondary control when there is a step change in load active power (P_L). At t = 0s, a 1kW load is introduced, and at t = 3.1s the load is turned off. In both cases, the secondary control restores the voltage within around 2s, while maintaining power sharing. As shown in the figure, the power sharing error of inverter 1 and 2, $P_{err\,(1,2)\,\%} \cong 0\%$. A similar scenario was also performed to test the response of the secondary control to a step change in reactive power (Q_L). Fig 22(b) shows the reactive powers supplied by each inverter, the load power and the frequency. In both cases of turning on and off the reactive load, the frequency was restored within around 8s. In this case, $Q_{err\,(1)\,\%} \cong 4\%$ and $Q_{err\,(2)\,\%} \cong 0.7\%$.

4.3.2 POWER LIMITATION

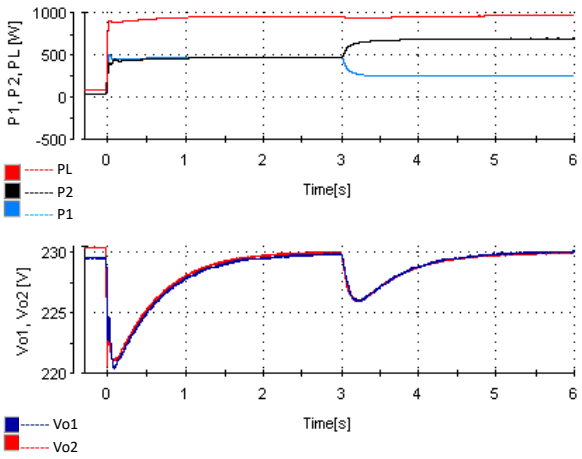
As already described, the power limitation controller can limit the output power of the converter depending on its operating conditions. To experimentally validate the operation of the active power limitation controller, two scenarios were considered. In the first case presented in Fig. 42(a), a step increase of active power (1kW) is introduced at t = 0s, with inverter 1 having its active power limited to 0.25kW and inverter 2 having no power limitation. The power supplied by inverter 2 is constrained only

by its capacity (1kVA). During a step increase in load, inverter 1 limits its output active power to 0.25kW, and the other inverter that has not yet reached its limit increases its output power to balance the load consumption. At t = 3.1s, the load is switched off. As shown in Fig 23(a), secondary control also restores voltage under active power limitation constraints. In the second case shown in Fig 23(b), the inverters are initially turned on with equal power sharing (no power limitation enforced). At t = 3s, P_{max} for inverter 1 is reduced to 0.25kW. As shown, inverter 1 limits its active output to P_{max}, while the remaining power is provided by inverter 2. Additionally, the results prove that secondary control restores the voltages during power limitation.

Similar scenarios are tested for the reactive power limitation controller, and the results are presented in Fig 24. In case 1, a step increase in reactive load is introduced at t = 0s, with inverter 1 having its reactive power limited to 0.1kVAr. As shown in Fig 24(a), inverter 1 limits its reactive power, and inverter 2 supplies the remaining load power. In case 2 shown in Fig 24(b), Q_{max} for inverter 1 is changed to 0.1kVAr at t = 10s. Its output power is reduced to 0.1kVAr demonstrating the ability of power limitation to control the power dispatched by the inverter. The results also demonstrate that the secondary control restores the frequency within 8s.

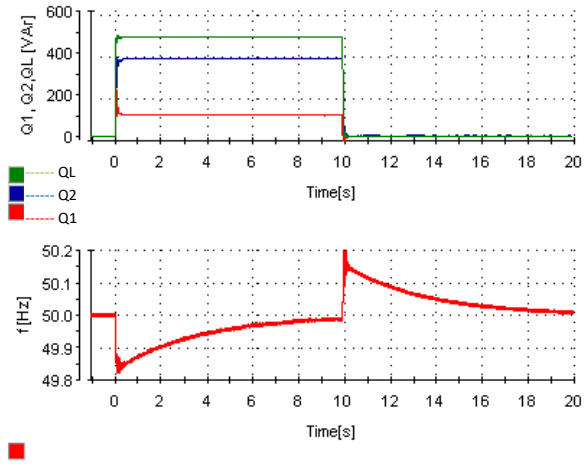


(a)

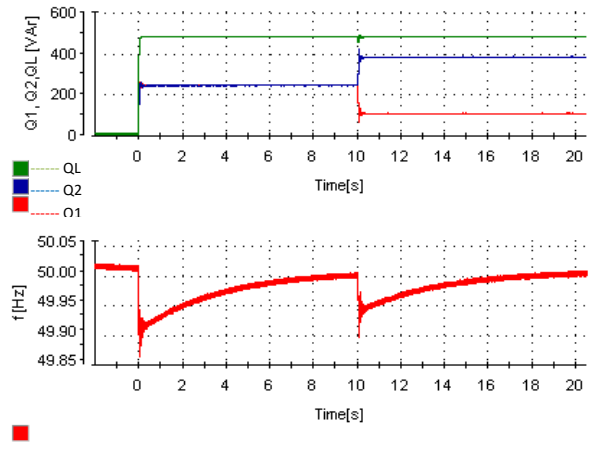


(b)

Fig 23. Active power limitation: (a) inverter 1 limited during start up; (b) inverters sharing equal power initially, then reduce P_{max} during operation.



(a)



(b)

Fig 24. Reactive power limitation: (a) inverter 1 limited during start up; (b) inverters sharing equal power initially, then reduce Q_{max} during operation.

4.4 CONCLUSION

The need to effectively control and manage diverse DERs necessitates more research on MG control strategies. To manage the intermittent nature of RES and the constraints posed by primary sources, this chapter presented a power limitation controller for VOC based inverters to dispatch power according to the operating conditions of the primary source. The controller successfully limited both the active and reactive power supplied by the inverters, which is essential for optimizing primary source's capacity utilization and preventing inverter overload. Furthermore, this thesis developed a secondary controller integrated with the VOC, designed to be robust against the effects of clock drifts in digital controllers. To this end, a decentralized secondary controller using a distributed averaging approach was implemented. The proposed controller restored the frequency and voltage to its nominal value while maintaining power sharing. Finally, an APD control was implemented in the VOC-based inverters to eliminate the low-frequency components in the DC-link. Various case scenarios were considered through simulations and experiments to analyze the performance of the proposed controllers.

5. ANDRONOV-HOPF- OSCILLATOR BASED CONTROL OF AN ISLANDED MG WITH DISTRIBUTED CONSENSUS SECONDARY CONTROL

The content of this chapter is part of a journal paper which has been submitted by the author for review to Electric Power Systems Research [104]. Furthermore, most of the research presented in this chapter, especially the experimental validation, was carried out during an Erasmus mobility at Aalborg University, Department of Energy Technology.

This chapter presents a consensus-based distributed secondary control framework designed to be compatible with AHO -based GFM inverters in islanded MGs. Compared to the Van der Pol oscillator, AHO demonstrated superior performance due to its ability to generate harmonics-free waveforms without compromising dynamic performance [100].

In previous studies, AHO has frequently been applied in three-phase systems due to its structure which inherently accepts two inputs, α-β components. However, in this thesis, AHO is adapted for single-phase systems by using a second order generalized integrator (SOGI) to generate β component from the measured inverter α current components. A state of the art, modelling and synchronization for the interconnected GFM inverters with the AHO control is provided in [101].

5.1 MICROGRID CONFIGURATION AND CONTROL

Fig 25 shows the proposed islanded MG consisting of three parallel single-phase voltage VSIs supplying a common load. The inverters are synchronized on a common AC bus, allowing coordinated power sharing. The inverter terminal outputs are connected to the common bus through LCL filter to mitigate harmonics introduced by inverter switching and to provide coupling impedance. Safe connection and disconnection of each inverter to the PCC was done through a circuit breaker. The primary control based on AHO oscillator and a consensus based distributed secondary control algorithms were programmed into a digital controller, which provides the switching signals to the inverters.

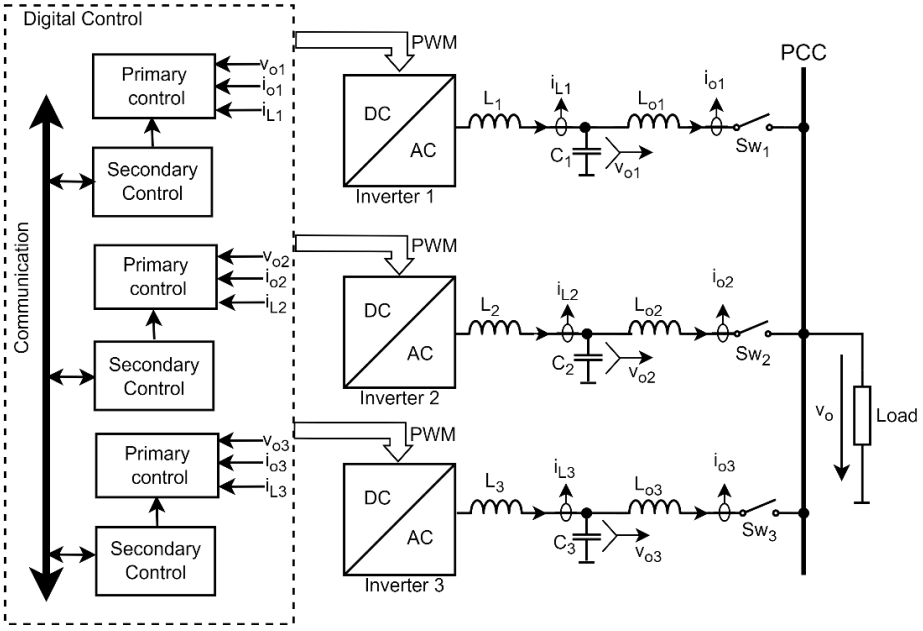


Fig 25. Proposed MG control structure with three parallel connected inverters.

5.1.1 ANDRONOV HOPF OSCILLATOR CONTROL

As depicted in Fig 26, AHO structure is composed of a resonant LC tank circuit oscillating with natural resonant frequency given by $\omega_n = 1/\sqrt{LC}$, where C and L are the virtual inductance and capacitance respectively. It also includes nonlinear, state-dependent voltage and current sources that sustain the oscillation. The interface between the inverter and AHO is provided through the voltage and current gain, k_v and k_i respectively. The dynamics of AHO can be expressed as a system of differential equations as shown in (28) and (29).

$$C\frac{dv_C}{dt} = -i_L + i_m - u_1 \tag{28}$$

$$L\frac{di_L}{dt} = -v_C + v_m - u_2 \tag{29}$$

The voltage across the virtual capacitor is denoted by v_C while i_L is the current through the virtual inductor. The inputs to the oscillator are denoted u_1 and u_2 while the non-linear voltage and current sources v_m and i_m that play a critical role in regulating the self-sustained oscillations is given by:

$$v_m = \frac{\xi}{\omega_{nom}}(2X_n^2 - x_1^2 - x_2^2)x_2 \tag{30}$$

$$i_m = \frac{\xi}{\varepsilon\omega_{nom}}(2X_n^2 - x_1^2 - x_2^2)x_1 \tag{31}$$

where ξ is speed constant that influences convergence speed to a steady state; X_n is the RMS amplitude and ε is the characteristic impedance given as $\varepsilon = \sqrt{L/C}$.

The state variables in (30), (31) can be defined as $x_1 = v_c$ and $x_2 = \varepsilon i_L$. The voltage references from the oscillator in $\alpha\beta$ frame can be produced by scaling the state variables with the voltage gain k_v as follows: $v_{\alpha\beta} = k_v[x_1, x_2]$.

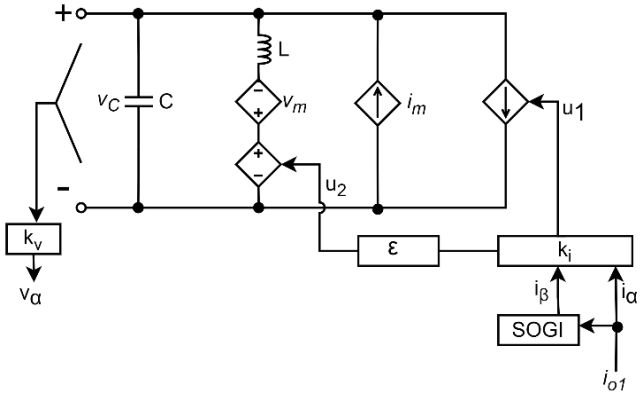


Fig 26. AHO control structure.

Substituting (30), (31) v_α and v_β into (28), (29) yields the following equations:

$$\frac{d\,v_\alpha}{dt} = \frac{\xi}{k_v^2}\left(2V_n^2 - v_\alpha^2 - v_\beta^2\right)v_\alpha - \omega_n v_\beta - \frac{k_v k_i}{C}i_\alpha \tag{32}$$

$$\frac{d\,v_\beta}{dt} = \frac{\xi}{k_v^2}\left(2V_n^2 - v_\alpha^2 - v_\beta^2\right)v_\beta + \omega_n v_\alpha - \frac{k_v k_i}{C} i_\beta \tag{33}$$

where $V_n = k_v X_n$ is the nominal RMS voltage.

The current scaling constants k_i for the inverter output current, which is used as feedback to the oscillator, is calculated as $k_i = V_n / S_{rated}$, while the voltage scaling factor is $k_v = V_n$.

A detailed design of the other parameters is provided in [102], and the values of the parameters used are presented in Table 13. The power sharing of the inverters satisfies the following condition [100]:

$$\frac{P_i}{P_j} = \frac{\varphi_i k_j}{\varphi_j k_i} \tag{34}$$

where k_i, k_j, and P_i, P_j ,and φ_i, φ_j are the current gains, active powers and power sharing ratios of the i^{th} and j^{th} inverter respectively.

5.1.2 CONSENSUS SECONDARY CONTROL

The application of consensus algorithm in distributed control is to ensure that state variables such as voltage and frequency of all DERs converge to a common value through an iterative process that involves the exchange of information among neighboring units. A typical consensus update rule is given by:

$$\frac{dx_i}{dt} = \sum_{j \in N_i} a_{ij}\left(x_j - x_i\right) \tag{35}$$

where a_{ij} are the adjacency matrix elements, x_i is the i^{th} agent state variable and N_i denotes a set of neighbors.

The proposed control relies on a fully distributed consensus approach to estimate the average voltage and frequency and converge all DERs to a common average as shown in (36) and (37). Each DER communicates its average estimate with its immediate neighbors to form a network-wide consensus that approximates the global state. Each DER then implements a local integral controller to drive its local voltage and frequency to nominal as shown in (38) and (39). To maintain power sharing among DERs, an additional term is included to preserve the power sharing defined by the primary control. This term is also calculated based on consensus, where DERs exchange normalized active and reactive power information with their neighbors to collectively adjust and maintain power sharing. The secondary control is implemented through the following equations.

$$V_i^{est}(t) = V_i(t) + \int_0^t \sum_{j \in N_i} a_{ij}\left(V_i^{est}(\tau) - V_j^{est}(\tau)\right)d\tau \tag{36}$$

$$\omega_i^{est}(t) = \omega_i(t) + \int_0^t \sum_{j \in N_i} a_{ij}\left(\omega_i^{est}(\tau) - \omega_j^{est}(\tau)\right)d\tau \tag{37}$$

$$\delta V_i(t) = K_{IV}\int_0^t (V_n - V_i^{est}(\tau))d\tau + K_{IP}\int_0^t \sum_{j \in N_i}\left(\frac{P_j^{nom}}{\varphi_j} - \frac{P_i^{nom}}{\varphi_i}\right)d\tau \tag{38}$$

$$\delta\omega_i(t) = K_{I\omega}\int_0^t (\omega_n - \omega_i^{est}(\tau))d\tau - K_{IQ}\int_0^t \sum_{j \in N_i}\left(\frac{Q_j^{nom}}{\varphi_j} - \frac{Q_i^{nom}}{\varphi_i}\right)d\tau \tag{39}$$

where V_i^{est} and ω_i^{est} are the network-wide the global state estimates while $\delta V_i(t)$ and $\delta\omega_i(t)$ are correction terms added to the primary control to restore the voltage and frequency. K_{IV}, $K_{I\omega}$, K_{IP}, K_{IQ} are the integrator constants. P_i^{nom} , P_j^{nom}, Q_i^{nom}, Q_j^{nom} are the normalized active and reactive powers of the i^{th} and j^{th} inverters respectively. φ_i and φ_j denotes the power sharing ratios.

Thus, the complete equations with both primary and secondary control could be written as follows:

$$\frac{d\,v_\alpha}{dt} = \frac{\xi}{k_v^2}\left(2(V_n - \delta V_i(t))^2 - v_\alpha^2 - v_\beta^2\right)v_\alpha - (\omega_n + \delta\omega_i(t))v_\beta - \frac{k_v k_i}{C} i_\alpha \tag{40}$$

$$\frac{d\,v_\beta}{dt} = \frac{\xi}{k_v^2}\left(2(V_n - \delta V_i(t))^2 - v_\alpha^2 - v_\beta^2\right)v_\beta - (\omega_n + \delta\omega_i(t))v_\alpha - \frac{k_v k_i}{C} i_\beta \tag{41}$$

Fig 27 shows the overall hierarchical control structure for a single inverter. All other inverters are controlled with a similar control structure, composed of AHO based primary control, and a consensus bases secondary control. A virtual impedance R_d was added to minimize power sharing mismatches due to different line impedances and also help on dampening oscillations [103].v_{sync} is used for inverter synchronization process which will be described later.

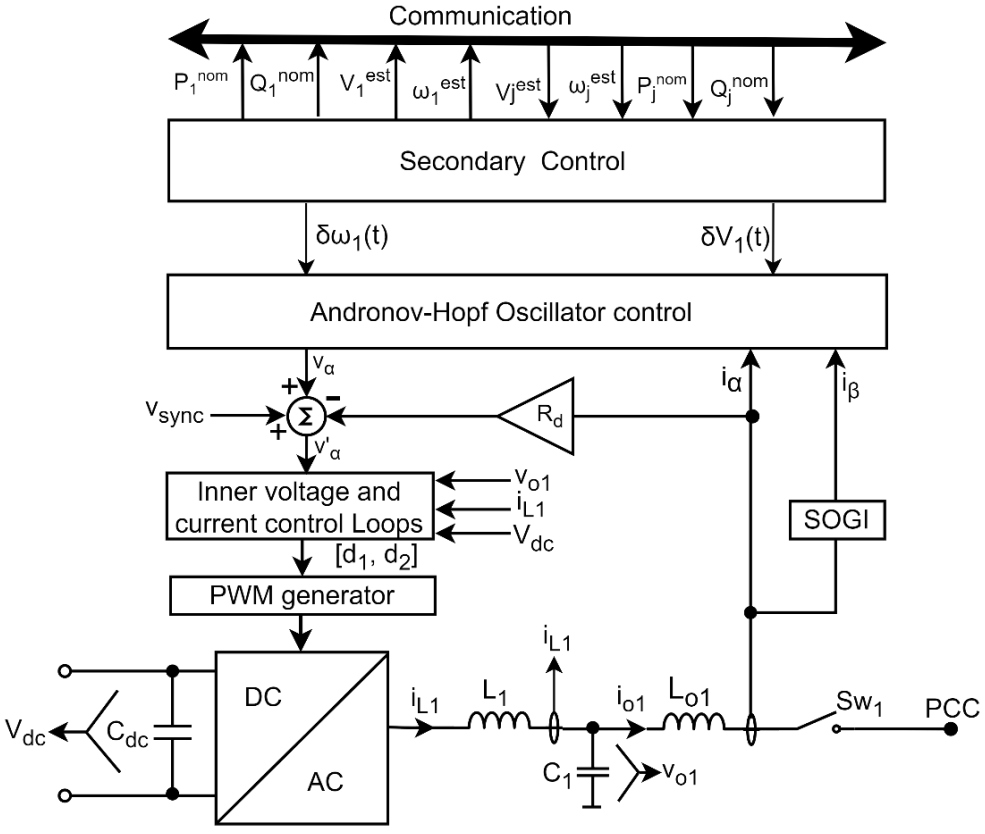


Fig 27. Overall structure of the proposed inverter control.

Table 13: Inverter and AHO parameter specifications.

Symbol	Description	Value
Inverter parameters		
S_{rated}	Rated apparent power	1k VA
V_n	Nominal RMS voltage	230 V
$V_{min,pu}$	Minimum voltage per unit	0.95
ω_n	Nominal angular frequency	2π50 rad/s
$\lvert\Delta\omega\rvert_{max}$	Maximum offset angular frequency	2π0.5 rad/s
L_o	Inverters side inductance	1.8 mH
L_g	Grid side inductance	1.8 mH
C_f	Filter capacitance	9 μF
V_{dc}	DC-link voltage	450 V
f_s	Switching frequency	10 kHz

5.2 EXPERIMENTAL RESULTS

To validate the proposed control method, two experimental setups (2 and 3), presented in Chapter 6, were implemented according to the structure presented in Fig 25 . The HIL setup was composed of DS 1006 dSPACE real-time platform and RT Box for executing the MG. Another setup was with physical inverters. The setup consists of three inverters, each with a rating of 1kW operating in single-phase configuration and a programmable DC power supply for powering the setup (the three inverters share a common DC bus). All the other parameters of the setup are presented in Table 13. Real time measurements were displayed and recorded through dSPACE ControlDesk. More details on the set-ups are provided in Chapter 6.

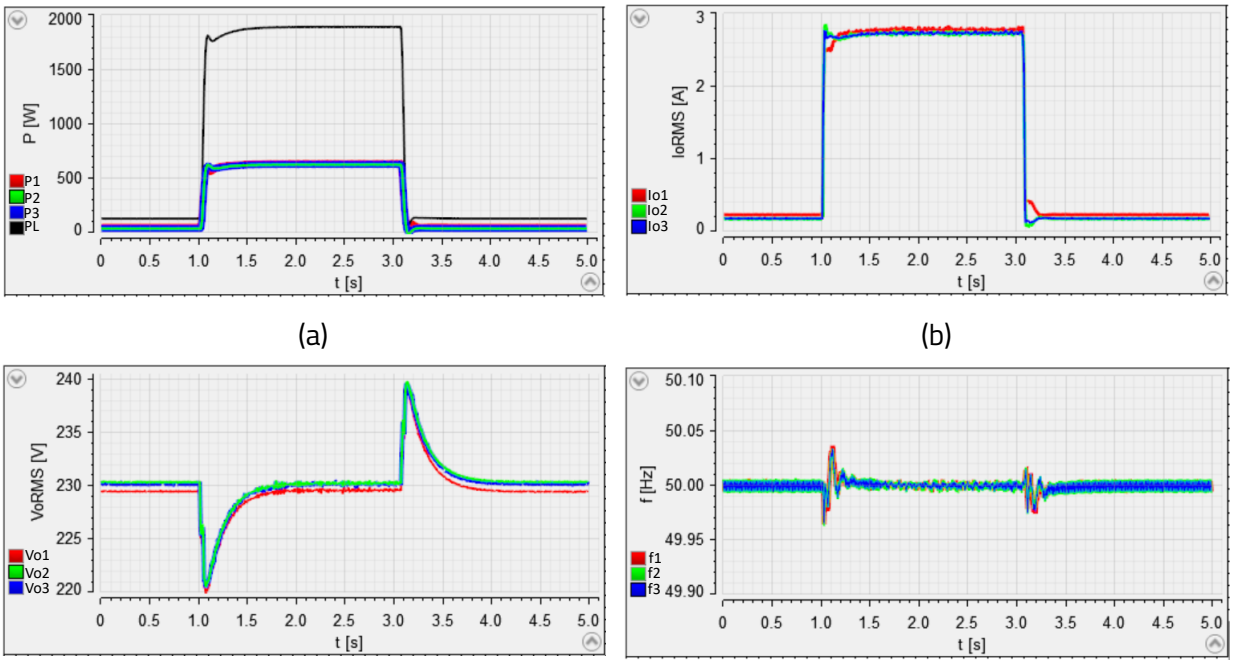
5.2.1 EXPERIMENTAL RESULTS WITH A PHYSICAL MG

After verifying the proposed control strategy through HIL experiments, further validation was conducted using real inverter hardware to assess the performance of the proposed controller in a real MG environment. The setup used is detailed in Chapter 6.3.

5.2.1.1 SECONDARY CONTROL

Case A: Step Change in Active Load

Fig 28 shows the active powers of the distributed generators, RMS current, RMS voltage and frequency respectively. Following a step change in active power demand (P_L = 1.9kW) at t = 1s and t = 3s, the secondary control restored the voltage to its nominal in 1s. At t = 3s the primary load was switched off, with only light load remaining connected to prevent circulating currents among DGs. Some coupling between active power and frequency can also be observed in Fig 28(d) resulting in some frequency oscillations after the load is switched on and off that damp quickly within 0.5s. In addition to restoring the voltage, the consensus approach also maintained power sharing among DGs under dynamic load conditions as shown in Fig 28(a).



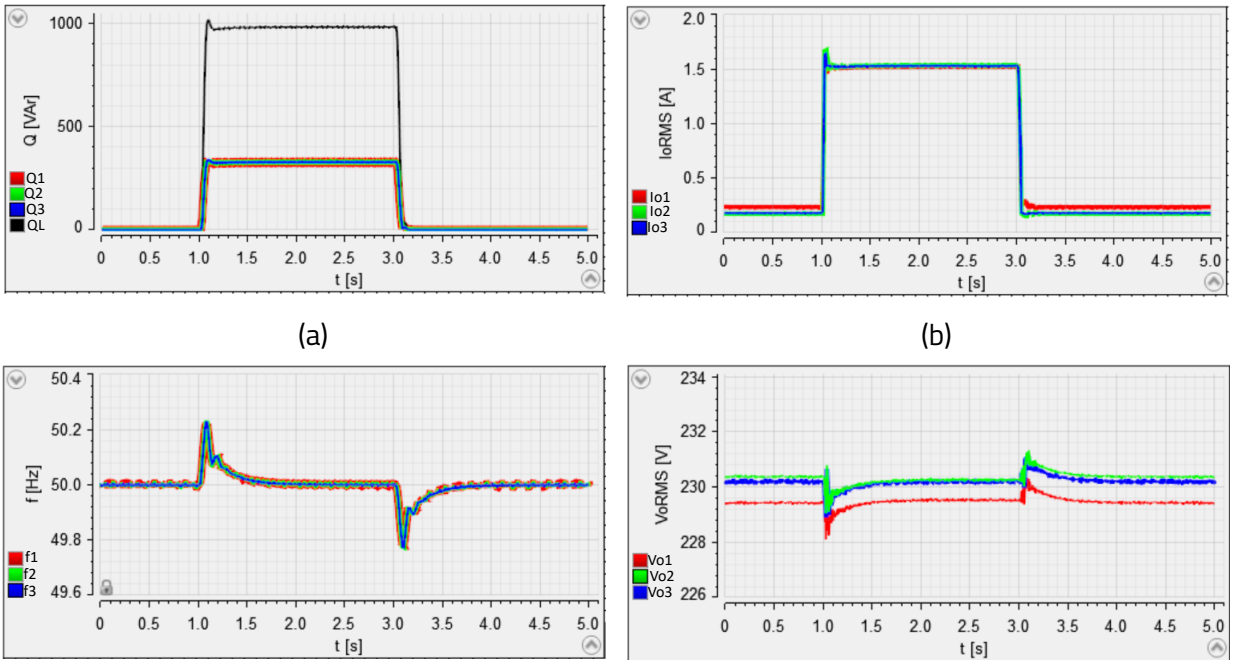
(a) (b)

(c) (d)

Fig 28. Step change in active power demand: (a) active power; (b) RMS current; (c) RMS voltage; (d) frequency.

Case B: Step Change in Reactive Load (Inductive)

In this case, the response of the secondary control was evaluated under a sudden change in reactive power demand (Q_L = 1kVAr). A reactive load was switched on at t = 1 s and switched off at t = 3s. Fig 29 shows the reactive powers of the distributed generators, RMS current demand, frequency and RMS voltage respectively.



(a) (b)

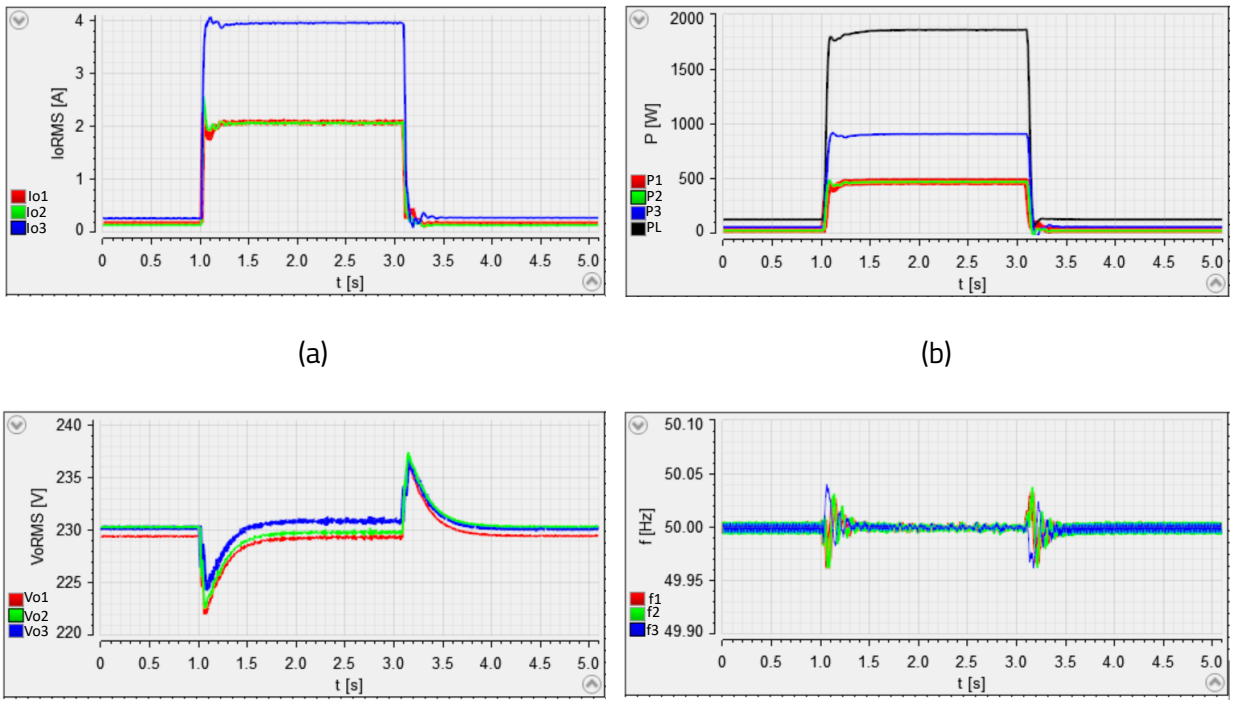
(c) (d)

Fig 29. Step change in reactive power demand: (a) reactive power; (b) RMS current; (c) frequency; (d) RMS voltage.

Following load connection, the frequency briefly overshoots to 50.24Hz and was restored to nominal in approximately 1 s. Similarly, following load disconnection the frequency was also restored to nominal in approximately 800ms. Secondary control also maintains reactive power sharing, before and after the system disturbance.

Case C: Step change in active load with unequal power sharing

In practice DGs may have unequal available power, and as such, units are expected to supply the load in proportion to their capacity to prevent overloading of smaller units. To reflect such conditions, the performance of the secondary control was analyzed under unequal current sharing ratio of 1: 1: 2. The experimental results are presented in Fig 30. A step change in active power demand was introduced at t = 1 s and at t = 3 s by connecting and disconnecting the load respectively. In both scenarios, the secondary control was able to restore the voltage to nominal within 1s. In addition, the power sharing ratio was also maintained before and after the disturbance.



(a) (b)

(c) (d)

Fig 30. Step change in active load (unequal power sharing): (a) RMS current; (b) active power; (c) RMS voltage; (d) frequency.

Case D: Secondary control considering communication delay

75ms communication delay

The communication delay was increased in discrete steps of 15ms. At 75ms more pronounced effects of the communication delay start to be observed on the current and active power. Inverters were added one after another following a procedure previously discussed and the added inverters oscillate. Fig 31 shows inverters active power outputs, reactive power, RMS output current, RMS output voltage and frequency respectively. Despite power oscillations, the consensus approach was able to restore the voltage and frequency following a step change in active and reactive power at t =1 and t = 3s. This

demonstrates the ability of the proposed consensus approach to be able to provide stable voltage and frequency control under moderate communication delays. However, when the delay was increased to 80ms, the system became unstable.

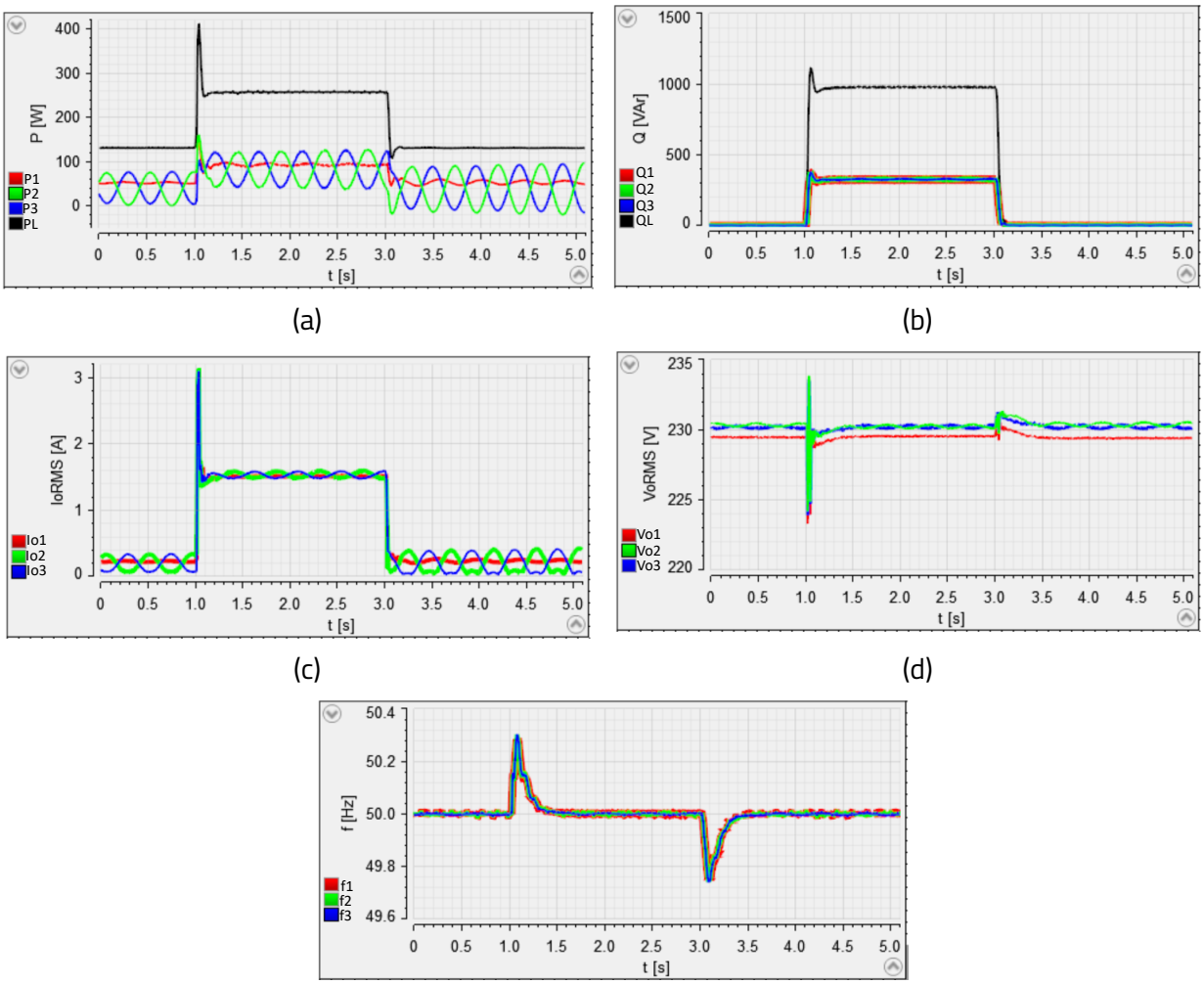


Fig 31. Step change in load power with 75ms communication delay: (a) active power; (b) reactive power; (c) RMS current; (d) RMS voltage; (e) frequency.

5.3 CONCLUSION

A consensus-based secondary control strategy integrated within a hierarchical control framework with AHO serving as the primary control in single-phase islanded MG has been implemented in this chapter. The consensus approach allows DGs to regulate both frequency and voltage as well as maintaining power sharing through local information exchange. Experimental validation was done using the dSPACE DS1006 control platform and three single-phase inverters. The experiments results demonstrated the effectiveness of the proposed strategy under various step changes in load power demand. The results also showed that the consensus approach restored voltage and frequency while maintaining power sharing under various operating conditions, which include equal and unequal power sharing, and different communication delay scenarios. Moreover, the system provided stable operations for moderate communication delays up to 75ms. At this delay, power oscillations were observed, while delays exceeding 75ms resulted in instability.

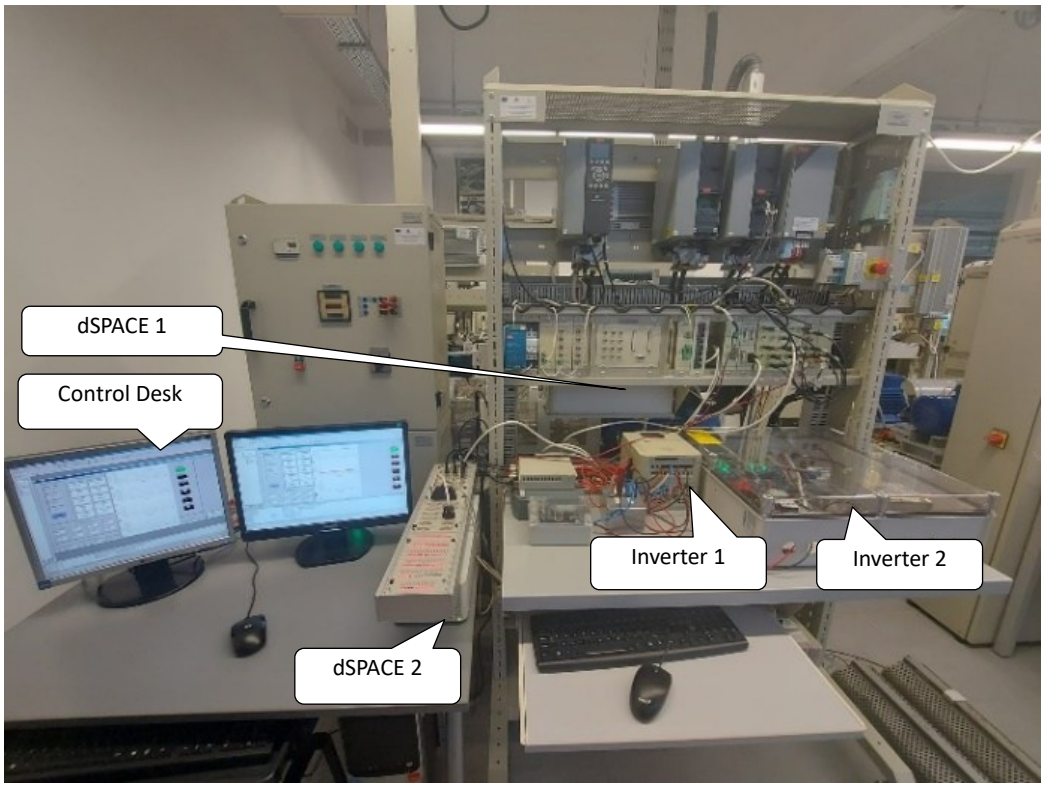
6. DEVELOPMENT OF EXPERIMENTAL PLATFORMS FOR MG APPLICATIONS

This chapter presents the experimental setups that were used throughout the thesis to support the development, validation, and testing of the proposed solutions. The first setup was developed at Transilvania University of Brasov/IDCT/L4 consisting of an MG platform comprised of two single-phase inverters. Control follows RCP using dSPACE 1103 for real-time implementation and testing. The second setup was developed at Aalborg University (AAU), PV systems laboratory equipped with dSPACE 1006 and RT Box hardware executing the MG model, enabling HIL implementation. The third setup was also done at AAU in MGs and Energy Internet Laboratory. The MG setup comprised of three single-phase inverters, and the control was provided by dSPACE. Detailed descriptions and configurations of these setups are provided in the subsequent subsections.

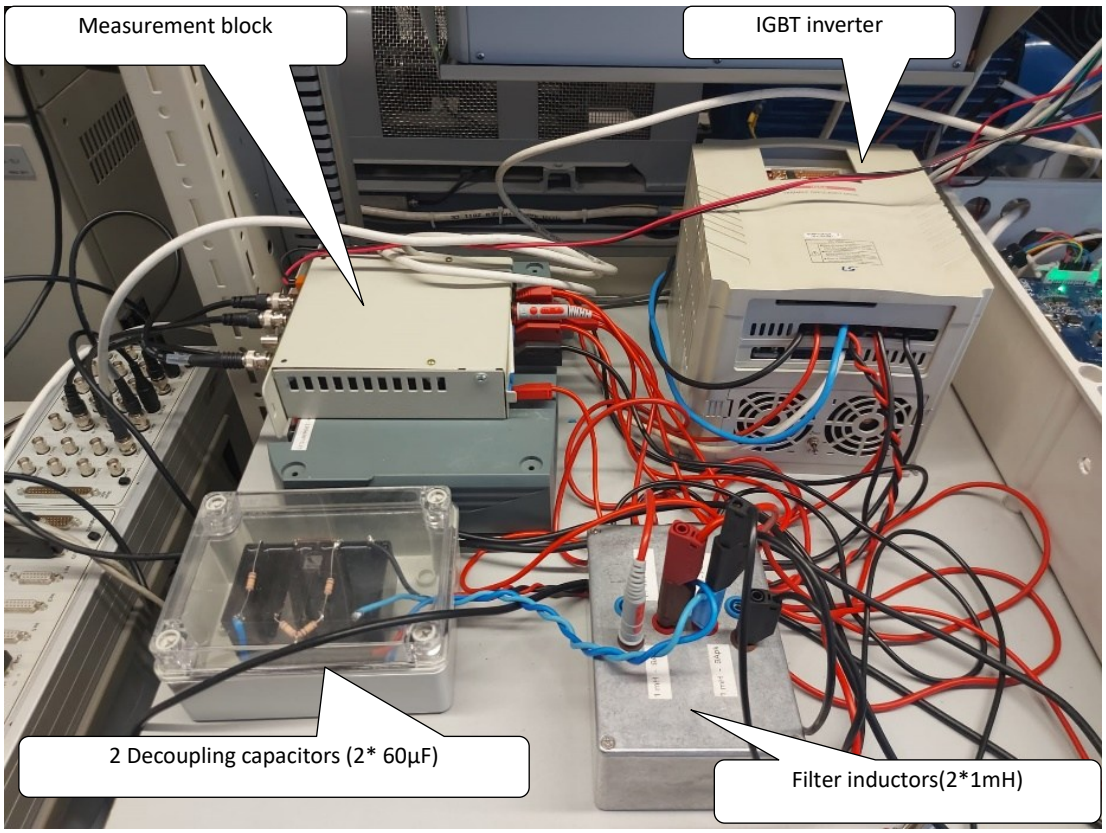
6.1 LABORATORY SETUP 1

6.1.1 HARDWARE AND CONTROL DEVELOPMENT

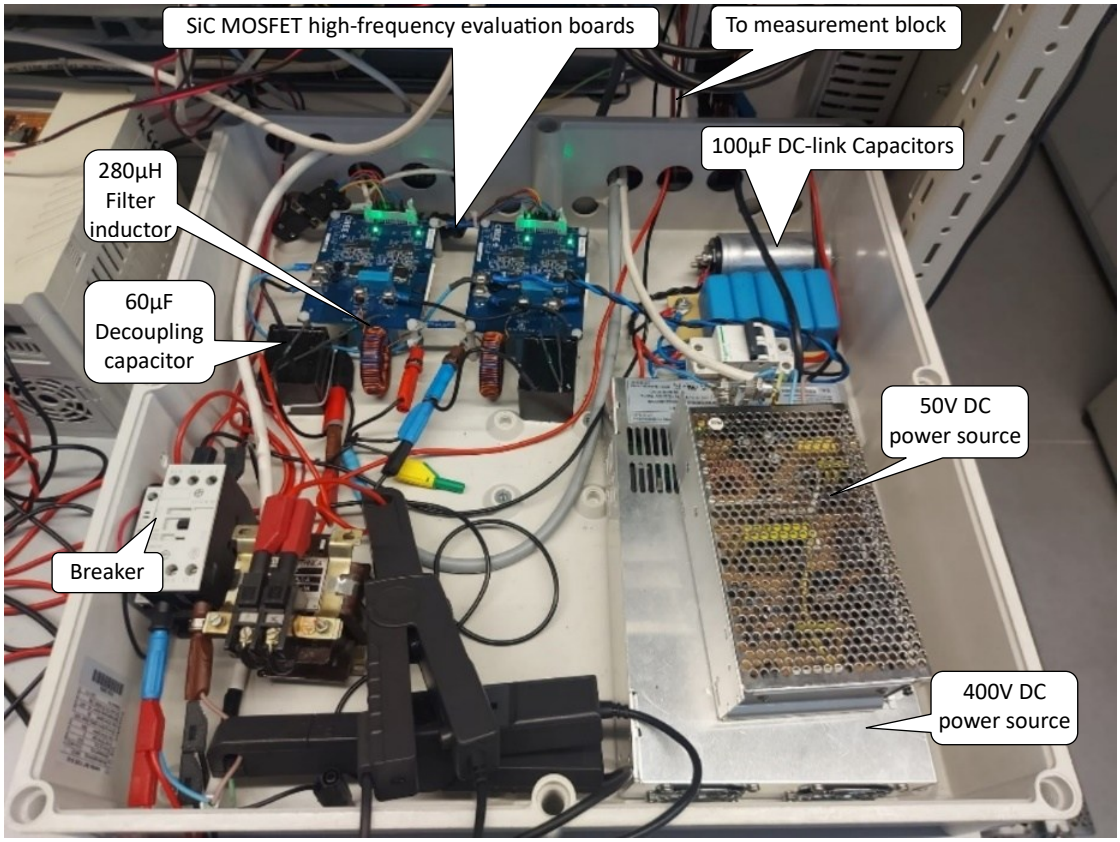
An experimental setup was built as shown in Fig 32 composed of two inverters. Each inverter was controlled by a separate dSPACE DS1103 controller, and the waveforms were acquired through ControlDesk software. DS1103 provides real time processing capabilities making it suitable for RCP.



(a)



(b)



(c)

Fig 32. Experiment: (a) hardware setup; (b) IGBT inverter; (c) SiC inverter.

6.2 LABORATORY SETUP 2

6.2.1 HARDWARE DE AND CONTROL DEVELOPMENT

The experimental setup shown in Fig 33 was designed to facilitate HIL testing of the developed MG control strategies. This setup was necessary as a preliminary stage before implementing the actual hardware, described in next section. This is part of PV systems laboratory at Aalborg University Department of Energy. The setup consists of dSPACE 1006 for real time control and PLECS RT Box for executing the model. The switching frequency of the inverters was 10kHz which aligned with the real inverter hardware specifications in setup 3. The MG model with three inverters was executed in RT box at a fixed step size of 5µs.

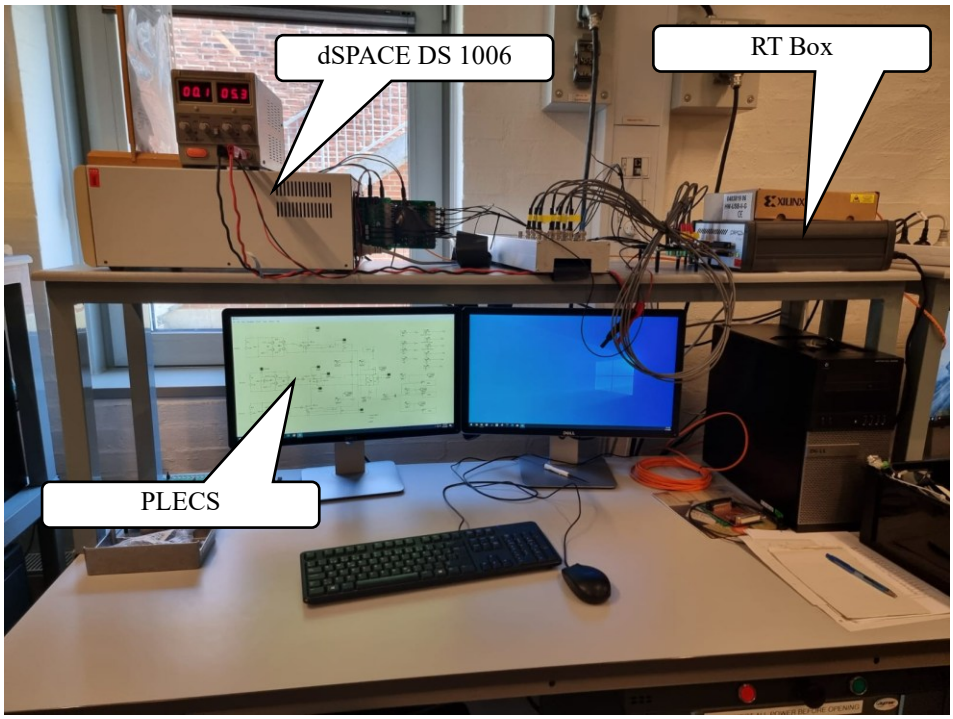


Fig 33. MG experimental test bench composed of PLECS, RTBox and dSPACE 1006.

6.3 LABORATORY SETUP 3

6.3.1 HARDWARE AND CONTROL DEVELOPMENT

The third experimental setup shown in Fig 34, consists of three Danfoss inverters physically interconnected to form a laboratory-scale MG supplying a common load. The setup follows the same structure as the previously described HIL configuration but uses real hardware on the MG power side. The control platform was also based on dSPACE 1006 real-time processor board following RCP framework. The control algorithms were modeled in MATLAB/Simulink and configured to run at a fixed sampling period of 100 µs. dSPACE ControlDesk was used for visualizing signals, acquiring data and parameter tuning.

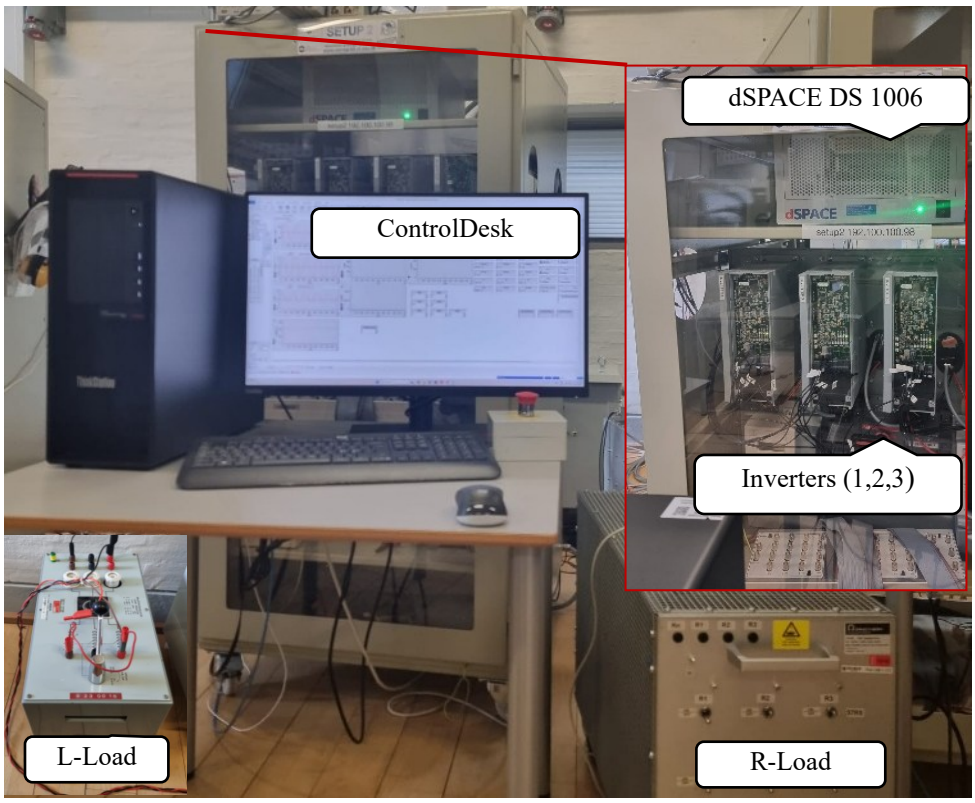


Fig 34. MG experimental test bench composed of 3 inverters and dSPACE 1006.

7. FINAL CONCLUSION

This thesis has presented advanced control strategies for single-phase inverters to enable their integration into MGs. The first part provided an extensive review of APD solutions for mitigating second-order oscillations inherent in DC-link of single-phase inverters and developed unified mathematical descriptions for differential inverters to derive an optimum topology considering different parameters. Single-phase inverters were subsequently integrated into MG systems using advanced control based on VOC, where two oscillators the Van der Pol oscillator and the Andronov–Hopf oscillator were implemented. Within VOC framework, a power-limitation controller was developed to enable the inverters to dispatch according to the operating conditions and the primary source availability. Two secondary control approaches based on distributed averaging and consensus protocol were formulated, for voltage and frequency restoration as well as maintaining power sharing among the inverters. Simulations and experimental platforms that include HIL testing and a laboratory MG with physical inverters were used to validate the proposed control methods.

7.1 SIGNIFICANCE AND BROADER IMPACT

The findings of this thesis hold significant value in the design and developments of single-phase inverters and their integration into MGs. The proposed and analyzed control methods that rely on APD help to improve the reliability and lifetime of single-phase inverters by offering a cost-effective method of replacing bulky electrolytic capacitors with more reliable film capacitors. This is because by redirecting the DC-link oscillations away from the DC-link, the capacitance requirements are reduced. This is particularly important in PV applications where typically inverters have a much shorter lifespan than PV panels. Extending inverter lifetime therefore reduces maintenance and replacement costs and improves overall system reliability. Furthermore, the findings are important in the context of the ongoing transformation of power systems driven by an increase in renewable-energy integration. In weak power grids, the need for advanced GFM control strategies has become critical to ensure stability, resilience, and reliable power delivery. By extending the emerging VOC framework, integrating power limitation and distributed secondary control schemes, this thesis advances a promising direction for the next generation of GFM inverters.

7.2 THESIS CONTRIBUTIONS

The main contribution of the thesis can be summarized as follows:

- Comprehensive state of the art analysis on differential single-phase inverters, providing main features, their operating principles and a comparative performance analysis in terms of the DC-link voltage requirements, losses, and stresses on the inverter components. Based on this analysis an optimum topology was derived.
- The development of unified mathematical description of the main differential single-phase inverter topologies, allowing an easier evaluation of their operational limits under different parameters.
- The thesis examined the main control strategies, applied to this class of inverters to achieve both primary control (autonomous or grid-connected operation) and APD functions, while advancing the development of control algorithms that are less dependent on parameter variations and more robust to external disturbances.

- Development and implementation of advanced VOC strategies on differential single-phase inverters for MGs integration, using both Van der Pol and Andronov–Hopf oscillator formulations. These control strategies provide fast synchronization, improved transient response and stable voltage and frequency regulation.
- Integration of VOC with APD techniques, establishing a unified control framework for single-phase inverters that removes second-order oscillations from the DC-link while maintaining stable GFM behavior.
- The development of power limitation method within the VOC framework, ensuring that inverters can dispatch power according to the operating conditions and primary source availability. The controller can limit both active and reactive power to specified setpoints. When an inverter reaches its power limit, the others that are not restricted by the power limitation take on the extra load.
- Formulation and implementation of distributed secondary-control strategies for oscillator-based MGs, employing a distributed-averaging method for the Van der Pol and a consensus-based protocol for the Andronov Hopf-oscillator VOC. These controllers enable voltage and frequency restoration and power sharing among the inverters. The secondary control methods were also designed to be robust to clock drifts, inherent in digital controllers.
- Validation of the proposed control strategies through real-time HIL testing, and experiments on a physical inverter-based MG demonstrating the practical feasibility under realistic operating conditions.

7.3 FUTURE RESEARCH DIRECTION

Building on the work presented in this thesis, several avenues for future research can be identified:

- A deeper understanding of how single-phase inverter topologies with APD schemes, which use a minimum number of semiconductors and result in slightly higher voltage and current stress, can maintain or even enhance reliability compared with traditional topologies. Combining reduced switch count topologies and the use of wide-bandgap semiconductors may prove to be an effective design approach.
- Developing advanced control algorithms that can effectively handle the high switching frequency of modern wide-bandgap transistors, which have now reached MHz frequencies (e.g. GaN devices), is a crucial task. Under such circumstances, methods that do not rely on PWM modulators while maintaining a constant frequency may prove to be the optimal solution. Moreover, as the switching frequency increases, the issue of leakage current becomes increasingly significant, particularly in PV applications.
- Analyzing how the APD circuit influences ancillary services, such inverters must provide. For example, one challenge is related to low-voltage ride-through capability, which is imposed in many grid codes today for grid-connected inverters. With a reduction in the DC capacitance, the APD-based inverters have less energy stored in the DC link to support riding through grid voltage sags. Further research is required to provide solutions to this issue.
- Future research could investigate the compatibility of VOC with established GFM control techniques such as droop control and VSM.
- A further promising direction is the exploration of artificial intelligence-based control strategies as potential alternatives or complements to oscillator-driven GFM control.

7.4 PUBLICATIONS ON THE DOCTORAL RESEARCH TOPIC

During the doctoral program we targeted high impact WOS journals (Q1/Q2) and IEEE international conferences, with most papers having me as the first author. This ensured that the work contributed to the peer-reviewed scientific literature.

Papers in WOS-indexed Journals

- **R. Musona** and I. Serban, "Control of a Single-Phase Islanded Microgrid Based on Virtual Oscillator Control Enhanced With Power Limitation and Robust Distributed Secondary Control," in *IEEE Open Journal of the Industrial Electronics Society*, vol. 6, pp. 25-42, 2025, doi: 10.1109/OJIES.2024.3519809. - Link
    - WOS Quartile: Q1;
    - WOS Impact Factor: 4.3
- **R. Musona** and I. Serban, "Differential Single-Phase Inverters With Active Power Decoupling: A Survey," in *IEEE Access*, vol. 11, pp. 53654-53670, 2023, doi: 10.1109/ACCESS.2023.3280228. – Link
    - WOS Quartile: Q2;
    - WOS Impact Factor: 3.6
- **R. Musona**, I. Serban, T. Kerekes, "Andronov-Hopf-Oscillator Based Control of an Islanded Microgrid With Distributed Consensus Secondary Control", submitted for review *to Electric Power Systems Research* –
    - WOS Quartile: Q2;
    - WOS Impact Factor: 4.2

Papers in IEEE International Conferences (indexed in IEEE Xplore / WOS)

- **R. Musona** and I. Serban, "Improving Microgrid Operation by Integrating Virtual Oscillator Control and Active Power Decoupling in Single-Phase Inverters", *2025 14th international conference on renewable energy research and applications (ICRERA),* Vienna, Austria, 2025, pp. 311-316, doi: 10.1109/ICRERA66237.2025.11283952.- Link
    - paper presented by the author at the conference in person.
    - Paper indexed in IEEE Xplore
- J. Sora, I. Serban, **R. Musona**, "Control of a DC MG Integrating a Single-Phase Inverter and a DAB for EV Charging and V2G Operation ", *2025 14th international conference on renewable energy research and applications (ICRERA),* Vienna, Austria, 2025, pp. 276-281, doi: 10.1109/ICRERA66237.2025.11284060.- Link
    - paper presented by the author at the conference in person.
    - Paper indexed in IEEE Xplore
- **R. Musona** and I. Serban, "Active Power Decoupling on a Differential Single-Phase Inverter With Non-linear Load," *2024 6th Global Power, Energy and Communication Conference (GPECOM)*, Budapest, Hungary, 2024, pp. 74-78, doi: 10.1109/GPECOM61896.2024.10582620. - Link
    - paper presented by the author at the conference in person.
    - paper indexed in IEEE Xplore and WOS.

- **R. Musona** and I. Serban, "A Comparative Performance Analysis Between the Buck and Boost Differential Single-Phase Inverters with Active Power Decoupling," *2023 International Aegean Conference on Electrical Machines and Power Electronics (ACEMP) & 2023 International Conference on Optimization of Electrical and Electronic Equipment (OPTIM)*, Istanbul, Turkiye, 2023, pp. 1-6, doi: 10.1109/ACEMP-OPTIM57845.2023.10287078. - Link
    - paper presented by the author at the conference in person.
    - Paper indexed in IEEE Xplore
- I. Serban and **R. Musona**, "A Single-Phase Reactive Power Compensator with Reduced-Size Film Capacitors and Active Power Decoupling Control," *2023 8th IEEE Workshop on the Electronic Grid (eGRID)*, Karlsruhe, Germany, 2023, pp. 1-5, doi: 10.1109/eGrid58358.2023.10380895. - Link
    - paper indexed in IEEE Xplore.

Papers published prior to the doctoral period in the field of the thesis:

- **R. Musona** and I. Serban, "A Comparative Analysis on a Single-Phase Inverter With a Reduced Component Count Power Decoupling Circuit," *2022 IEEE 20th International Power Electronics and Motion Control Conference (PEMC)*, Brasov, Romania, 2022, pp. 333-338, doi: 10.1109/PEMC51159.2022.9962863. - Link
    - paper presented by the author at the conference in person.
    - Paper indexed in IEEE Xplore and WOS
- **R. Musona** and I. Serban. "Comparative efficiency analysis between a conventional single-phase inverter and an inverter with a minimalist active power decoupling circuit." *Bulletin of the Transilvania University of Brasov. Series I-Engineering Sciences* (2022): 1-8, doi: doi.org/10.31926/but.ens.2022.15.64.1.1 (BDI journal) - Link

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